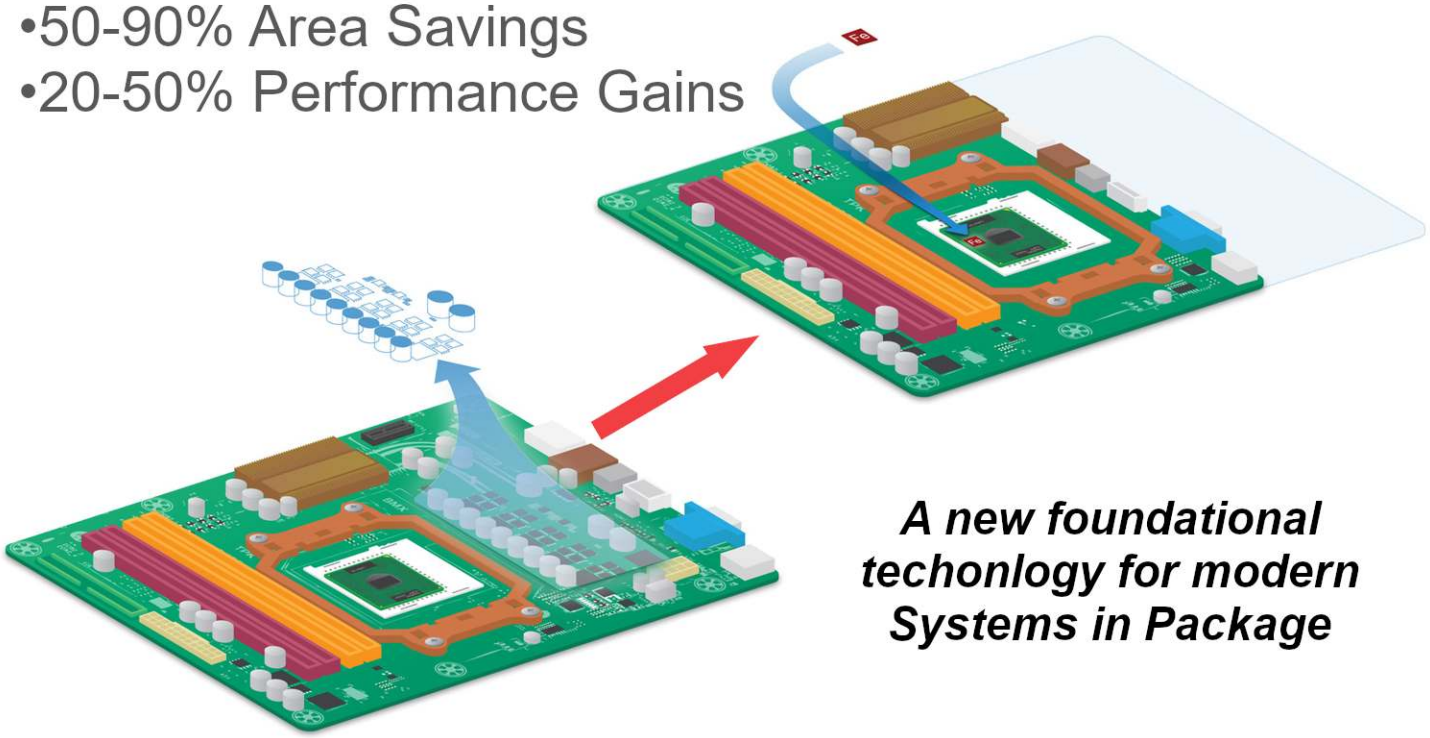
Ferric Product Brochure

Ferric's manufacturing and system technology facilitates integrated power management, enabling...

- 20-50% Power Savings
- 50-90% Area Savings
- 20-50% Performance Gains



A new foundational techonlogy for modern Systems in Package

Table 1: Product Table.

Part Number	Type	Phases	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	Efficiency
Fe1512	Buck	18	1.6-2.0	0.25-1.4	0-30	>90%
Fe1515	Buck	18	1.6-2.0	0.25-1.4	3, 3, 10, 13	>90%
Fe1810	Buck-Boost	4	1.6-2.0	0.9-2.0	2x 0-3.3	>90%
Fe4010	Buck	4	1.6-2.0	0.25-1.4	4x 0-1	>90%
Fe1508	Buck	12	1.6-2.0	0.25-1.4	0-20	>90%
Fe1038	Buck	8	1.8-2.5	0.6-1.5	0-3	>80%

30A, 18-phase DC-DC Step-Down Power Converter Chiplet with Integrated Ferromagnetic Inductors and PMBus Digital Interface

1 Features

- 18 phase buck converter with fully integrated power switches and thin film ferromagnetic power inductors
- Efficiency >90%
- Input Voltage Range: 1.6V - 2.0V
- Output Voltage Range: 0.25V - 1.4V
- High Switching Frequency: 180MHz
- Wide Loop Bandwidth: 50MHz
- Output Voltage Ripple: <1mVp-p at full load
- True Point-of-Load (PoL) Sensing
- 1MHz PMBus-Compliant Serial Interface
- 50MHz AVSBus-Compliant Serial Interface enabling Dynamic Voltage Scaling (DVS)
- Gang Operation
- Automatic Phase Shedding
- Input Voltage, Output Voltage, Output Current and Temperature Telemetry
- UVLO, OVP, OCP, and OTP Fault Response
- 19mm^2 footprint

2 Applications

- High performance multi-core systems-on-chip
- GPUs, TPUs, ASICs and FPGAs
- Data center processors
- Embedded industrial systems

3 Performance

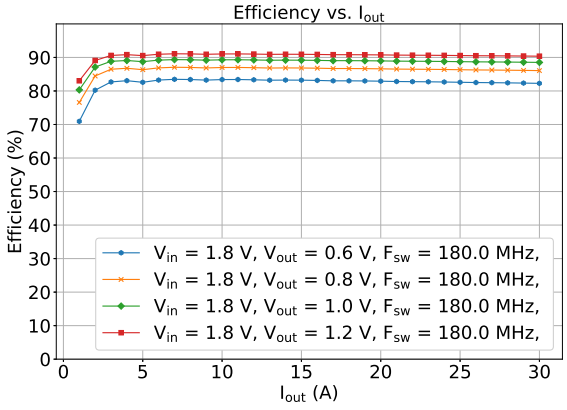


Figure 1: Efficiency vs I_{OUT} for V_{IN}=1.8V.

4 General Description

The Fe1512, Power System on a Chip (PwrSoC), is an 18-phase interleaved buck converter with fully integrated powertrain, including thin-film ferromagnetic power inductors. The Fe1512 integrates digital interface, power management, voltage control and powertrain circuitry (including power FETs, inductors and capacitors) all in one die. The Fe1512's precise voltage, fast transient, high bandwidth regulation, coupled with high switching frequency powertrain driving Ferric's magnetic composite integrated inductor technology, deliver high efficiency, high-quality power in a small footprint and volume to reduce board area, layout complexity, and Bill of Material (BOM).

5 Typical Package Footprint

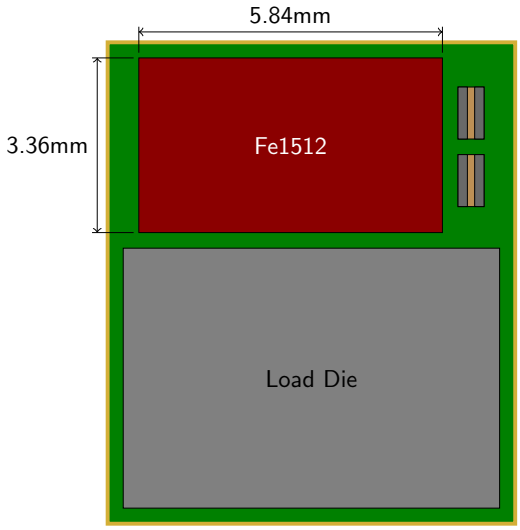


Figure 2: Typical package footprint.

6 Contact Information

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7 Electrical Specifications

In Table 1, V_{IN} = AVDD18 = VDDIO = 1.8V, V_{OUT}=0.9V, T_J=[-40,125]°C. Typical values are at T_J=25°C.

Table 1: Electrical specifications.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN Voltage Range	V_{IN}	AVDD18 $\geq$ V_IN	1.6	1.8	2.0	V
Output Voltage Range	V_{OUT}	$V_{IN} \geq$ 1.8V	0.25		1.4	V
Output Voltage Resolution	$V_{OUT,RES}$			1.7		mV
Steady State Output Current	I_{OUT}				30	A
Number of Powertrain Phases	N_{PHASES}		2		18	Phases
DC Line Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Line}$	V_{IN}=[1.6,2.0]V		$\pm$ 0.5		%
DC Load Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Load}$	I_{OUT}=[0,30]A		$\pm$ 0.5		%
Output Voltage Ripple	ΔV_{RIPPLE}	$C_{LOAD} \geq$600nF		1		mV
Switching Frequency	f_{SW}		100	180	200	MHz
Load Current Step Up Response	$\lvert\Delta V_{OUT,UP}\rvert$	ΔI : 8A to 23A Δ t = 2ns C_{LOAD}=600nF		80		mV
Load Current Step Down Response	$\lvert\Delta V_{OUT,DN}\rvert$	ΔI : 23A to 8A Δ t = 2ns C_{LOAD}=600nF		80		mV

8 Application Schematic

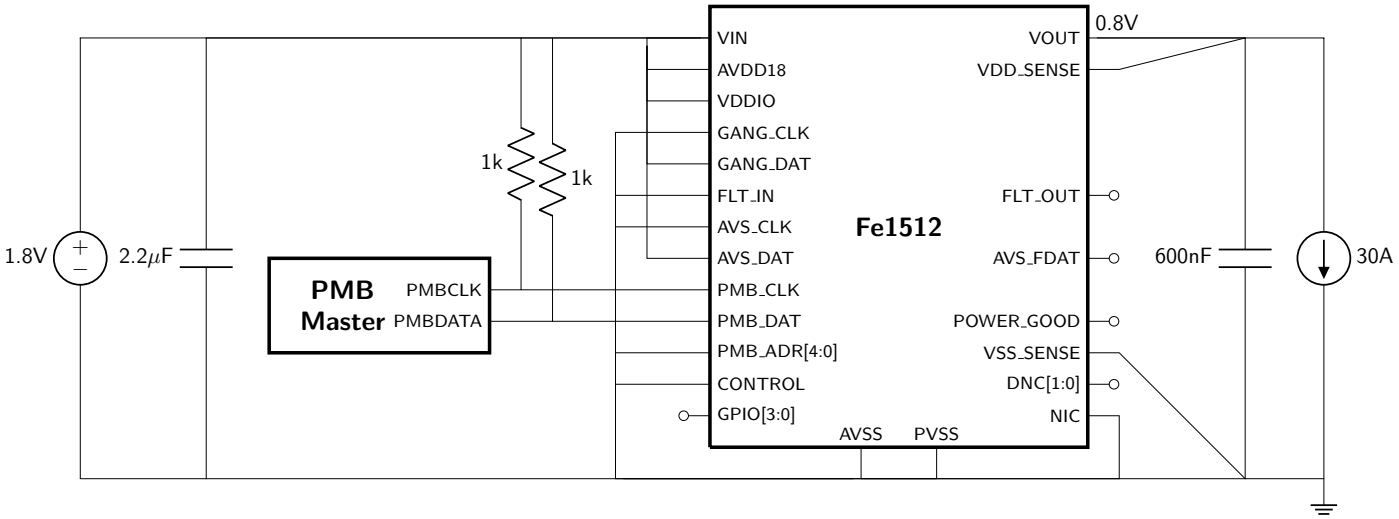

Figure 3: Application schematic for single chip operation with PMBus Interface.

Multiple Output (13A, 10A, 3A, 3A) DC-DC Step-Down Power Converter Chiplet with Integrated Ferromagnetic Inductors

1 Features

- Multi-output buck converter with fully integrated power switches and thin film ferromagnetic power inductors
- Output current per domain: 13A, 10A, 3A, 3A
- Efficiency: 90%
- Input Voltage Range: 1.6V - 2.0V
- Output Voltage Range: 0.25V - 1.4V
- High Switching Frequency: 180MHz
- Wide Loop Bandwidth: 50MHz
- True Point-of-Load (PoL) Sensing
- 1MHz PMBus Compliant Serial Interface
- 50MHz AVSBus Compliant Serial Interface enabling Dynamic Voltage Scaling (DVS)
- Automatic Phase Shedding on 13A domain
- Input Voltage, Output Voltage, Output Current and Temperature Telemetry
- UVLO, OVP, OCP, and OTP Fault Response
- 20mm^2 footprint

2 Applications

- High Bandwidth Memory
- High performance multi-core systems-on-chip
- GPUs, TPUs, ASICs and FPGAs
- Embedded industrial systems

3 Contact Information

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4 General Description

The Fe1515, Power System on a Chip (PwrSoC), is a multiple output buck converter with fully integrated powertrain, including thin-film ferromagnetic power inductors. The Fe1515 integrates digital interface, power management, voltage control and powertrain circuitry (including power FETs, inductors and capacitors) all in one die. The 18 total powertrain phases on the design are connected as appropriate for the four output domains with unique current handling capabilities: 8 phases are allocated for the 13A domain, 6 phases are allocated for the 10A domain, and 2 phases are allocated for each 3A domain. The Fe1515's precise voltage, fast transient, high bandwidth regulation, coupled with high switching frequency powertrain driving Ferric's magnetic composite integrated inductor technology, deliver high efficiency, high-quality power in a small footprint and volume to reduce board area, layout complexity, and Bill of Material (BOM).

5 Typical Package Footprint

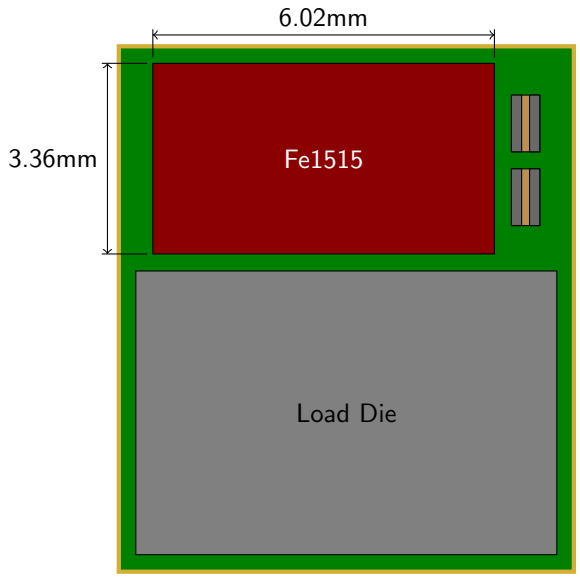

Figure 1: Typical package footprint.

6 Electrical Specifications

In Table 1, V_{IN} = AVDD18 = VDDIO = 1.8V, V_{OUT}=0.9V, T_J=[-40,125]°C. Typical values are at T_J=25°C.

Table 1: Electrical specifications.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN Voltage Range	V_{IN}		1.6	1.8	2.0	V
Output Voltage Range	V_{OUT}	$V_{IN} \geq$ 1.8V	0.25		1.4	V
Output Voltage Resolution	$V_{OUT,RES}$			1.7		mV
DC Line Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Line}$	1.6V $\leq V_{IN} \leq$ 2.0V		$\pm$ 0.5		%
DC Load Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Load}$			$\pm$ 0.5		%
Steady State Output Current 0	$I_{OUT,0}$				13	A
Number of Powertrain Phases 0	$N_{PHASES,0}$		2		8	Phases
Steady State Output Current 1	$I_{OUT,1}$				10	A
Number of Powertrain Phases 1	$N_{PHASES,1}$		2		6	Phases
Steady State Output Current 2	$I_{OUT,2}$				3.4	A
Number of Powertrain Phases 2	$N_{PHASES,2}$		2		2	Phases
Steady State Output Current 3	$I_{OUT,3}$				3.4	A
Number of Powertrain Phases 3	$N_{PHASES,3}$		2		2	Phases
Switching Frequency??	f_{SW}		100	180	200	MHz

7 Application Schematic

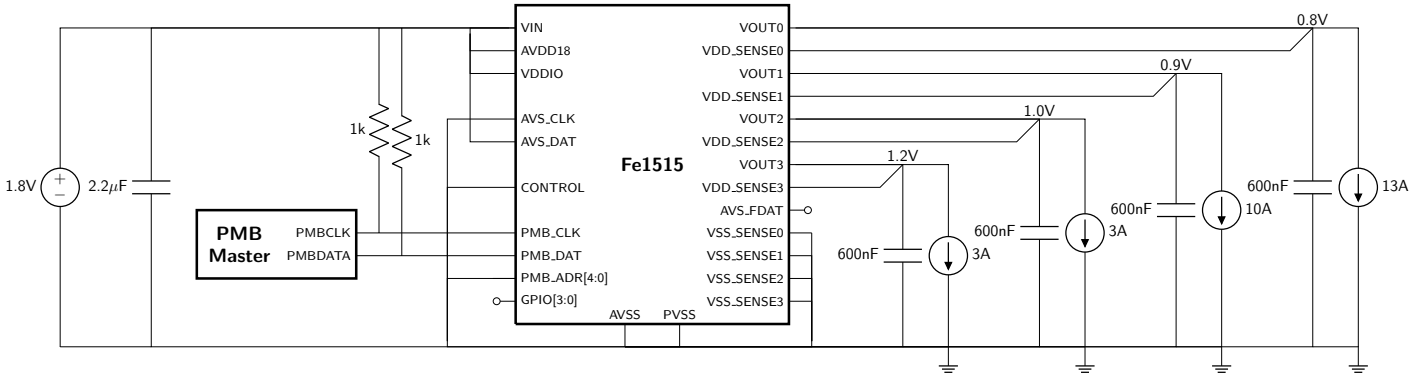

Figure 2: PMBus interface application schematic.

6A, 4-phase DC-DC Non-Inverting Buck-Boost Converter Chiplet with PMBus Digital Interface

1 Features

- Non-inverting Buck-Boost converter
- Integrated power switches
- Optionally multi-output
- 4 powertrain phases
- Automatic Transitioning between Buck Mode and Boost Mode
- Efficiency: >90%
- Input Voltage Range: 1.6V - 2.0V
- Output Voltage Range: 1.6V - 2.0V
- High Switching Frequency: 120MHz
- Wide Loop Bandwidth: 20MHz
- Output Voltage Ripple: <1mVp-p at full load
- True Point-of-Load (PoL) Sensing
- 1MHz PMBus-Compliant Serial Interface
- 50MHz AVSBus-Compliant Serial Interface enabling Dynamic Voltage Scaling (DVS)
- Gang Operation
- Automatic Phase Shedding
- Input Voltage, Output Voltage, Output Current and Temperature Telemetry
- UVLO, OVP, OCP, and OTP Fault Response
- 11mm^2 solution footprint

2 Applications

- FPGAs
- RF Systems in Package
- IO Domains

3 Contact Information

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4 General Description

The Fe1810, Power System on a Chip (PwrSoC), is a 4-phase interleaved non-inverting buck-boost converter intended for conversion ratios approximately equal to 1. The Fe1810 's outputs (VOUT0 and VOUT1) can be configured to operate in parallel or as two distinct output domains. The Fe1810 achieves high efficiency by operating in either buck mode or boost mode and transitioning between the two automatically. The Fe1810 integrates digital interface, power management, voltage control and powerFETs all in one die. Using the FeL1801 Integrated Passive Device (IPD) with the Fe1810 leads to dense solution sizes. The Fe1810's precise voltage, fast transient, high bandwidth regulation, coupled with high switching frequency powertrain driving Ferric's magnetic composite integrated inductor technology, deliver high efficiency, high-quality power in a small footprint and volume to reduce board area, layout complexity, and Bill of Material (BOM).

5 Typical Package Footprint

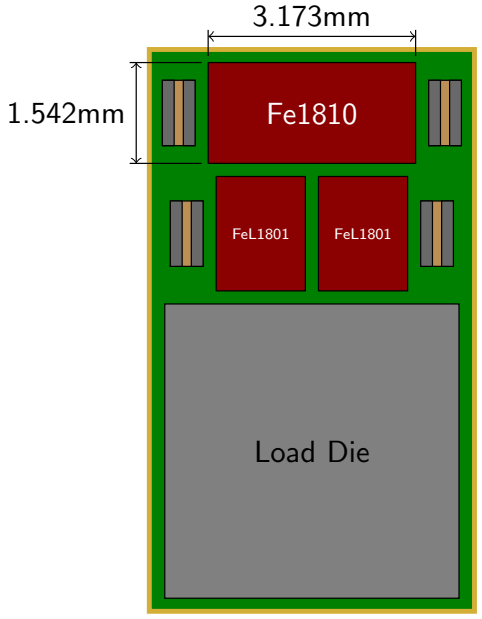

Figure 1: Typical package footprint.

6 Electrical Specifications

In Table 1, V_{IN} = AVDD18 = VDDIO = 1.8V, V_{OUT}=1.8V, T_J=[-40,125]°C. Typical values are at T_J=25°C.

Table 1: Electrical specifications.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN Voltage Range	V_{IN}	AVDD18 $\geq$ V_IN	1.6	1.8	2.0	V
Output Voltage Range	V_{OUT0}, V_{OUT1}		1.6		2.0	V
Output Voltage Resolution	$V_{OUT,RES}$			3.4		mV
Steady State Output Current	I_{OUT}				6.4	A
Number of Powertrain Phases	N_{PHASES}		2		4	Phases
DC Line Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Line}$			$\pm$ 0.5		%
DC Load Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Load}$			$\pm$ 0.5		%
Output Voltage Ripple	ΔV_{RIPPLE}	$C_{LOAD}\geq$600nF		1		mV
Switching Frequency	f_{SW}		80	120	160	MHz
Load Current Step Up Response	$\lvert\Delta V_{OUT,UP}\rvert$	ΔI : 1A to 10A Δ t = 2ns C_{LOAD}=600nF		80		mV
Load Current Step Down Response	$\lvert\Delta V_{OUT,DN}\rvert$	ΔI : 10A to 1A Δ t = 2ns C_{LOAD}=600nF		80		mV

7 Application Schematics

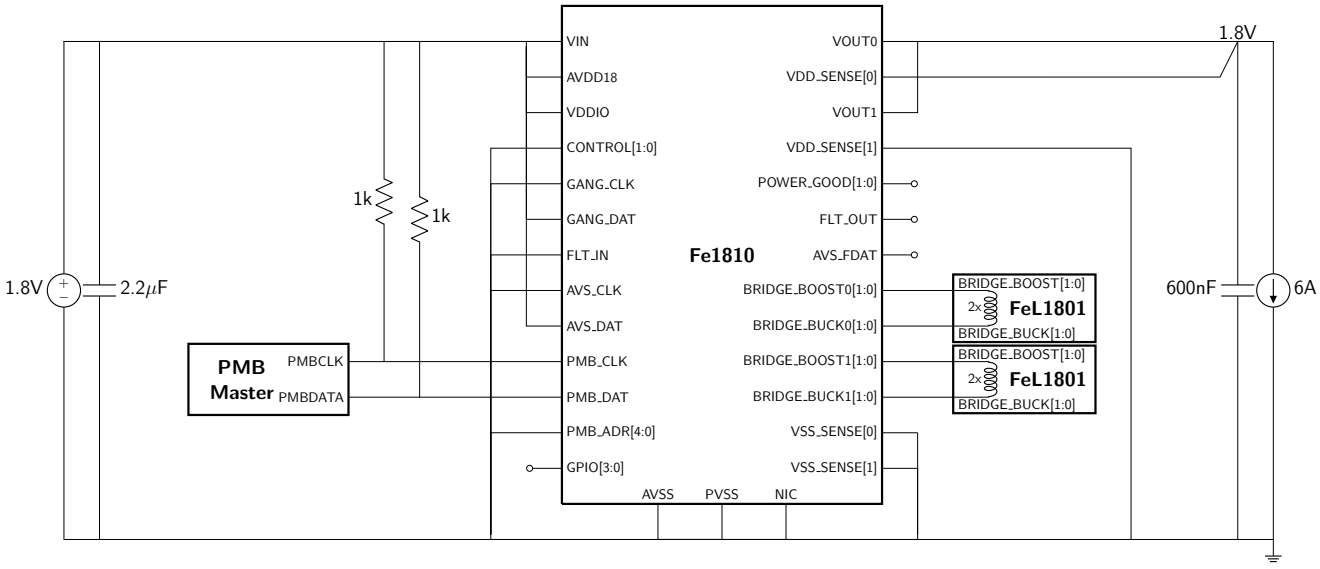

Figure 2: PMBus interface application schematic for 1 VOUT rail.

Multiple Output DC-DC Step-Down Power Converter Chiplet with Integrated Ferromagnetic Inductors

1 Features

- Integrated power switches
- Integrated thin film ferromagnetic inductors
- Four independent output domains
- Output current per domain: 1A
- Efficiency: 90%
- Input Voltage Range: 1.6V - 2.0V
- Output Voltage Range: 0.25V - 1.4V
- Pulse Frequency Modulation Control
- True Point-of-Load (PoL) Sensing
- 1MHz PMBus Compliant Serial Interface
- 50MHz AVSBus Compliant Serial Interface enabling Dynamic Voltage Scaling (DVS)
- Input Voltage, Output Voltage, Output Current and Temperature Telemetry
- UVLO, OVP, OCP, and OTP Fault Response
- 11mm^2 footprint

2 Applications

- Low power FPGAs
- Internet-of-Things Devices

3 General Description

The Fe4010, Power System on a Chip (PwrSoC), is a multiple output buck converter with fully integrated powertrain, including thin-film ferromagnetic power inductors. The Fe4010 integrates digital interface, power management, voltage control and powertrain circuitry (including power FETs, inductors and capacitors) all in one die. Each of the four powertrain phases is regulated by independent controllers, allowing for 4 unique output domains. Each output domain can support up to 1A of sustained output current. The Fe4010's precise voltage, fast transient, high bandwidth regulation, coupled with high switching frequency powertrain driving Ferric's magnetic composite integrated inductor technology, deliver high efficiency, high-quality power in a small footprint and volume to reduce board area, layout complexity, and Bill of Material (BOM).

4 Typical Application Diagram

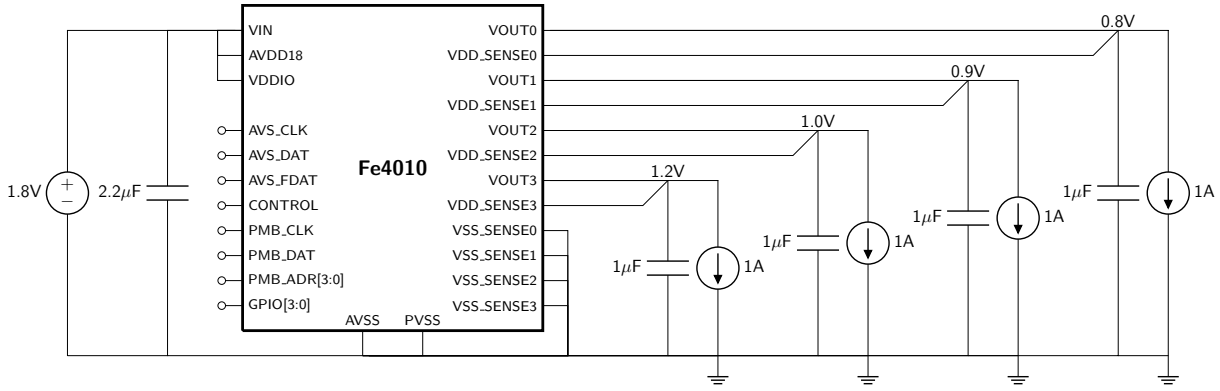

Figure 1: Typical application schematic.

5 Electrical Specifications

In Table 1, V_{IN} = AVDD18 = VDDIO = 1.8V, V_{OUT}=0.9V, T_J=[-40,125]°C. Typical values are at T_J=25°C.

Table 1: Electrical specifications.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Supply						
VIN Voltage Range	VIN		1.6	1.8	2.0	V
AVDD18 Non-Switching Quiescent Current	$I_{NS,AVDD18}$	Output Disabled		1080		µA
VIN Non-Switching Quiescent Current	$I_{NS,VIN}$	Output Disabled		790		µA
Output Voltage Range	V_{OUT}	$V_{IN} \geq$ 1.8V	0.25		1.4	V
Output Voltage Resolution	$V_{OUT,RES}$			1.7		mV
Steady State Output Current	$I_{OUT,0}$				1	A
Output Voltage Ripple	ΔV_{RIPPLE}	$C_{LOAD} \geq$600nF		1		mV
DC Line Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Line}$			± 0.5		%
DC Load Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Load}$			± 0.5		%
Dynamic Characteristics for Each Domain						
Load Current Step Up Response	$\lvert\Delta V_{OUT0,UP}\rvert$	Δ I : 1mA to 1A Δ t = 1ns C_{LOAD} = 500nF		100		mV
Load Current Step Down Response	$\lvert\Delta V_{OUT0,DN}\rvert$	Δ I : 1A to 1mA Δ t = 1ns C_{LOAD} = 500nF		100		mV

6 Contact Information

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20A, 12-phase DC-DC Step-Down Power Converter Chiplet with Integrated Ferromagnetic Inductors and PMBus Digital Interface

1 Features

- 12 phase buck converter with fully integrated power switches and thin film ferromagnetic power inductors
- Efficiency >90%
- Input Voltage Range: 1.6V - 2.0V
- Output Voltage Range: 0.25V - 1.4V
- High Switching Frequency: 180MHz
- Wide Loop Bandwidth: 50MHz
- Output Voltage Ripple: <1mVp-p at full load
- True Point-of-Load (PoL) Sensing
- 1MHz PMBus-Compliant Serial Interface
- 50MHz AVSBus-Compliant Serial Interface enabling Dynamic Voltage Scaling (DVS)
- Gang Operation
- Automatic Phase Shedding
- Input Voltage, Output Voltage, Output Current and Temperature Telemetry
- UVLO, OVP, OCP, and OTP Fault Response
- 14mm^2 footprint

2 Applications

- High performance multi-core systems-on-chip
- GPUs, TPUs, ASICs and FPGAs
- Data center processors
- Embedded industrial systems

3 Performance

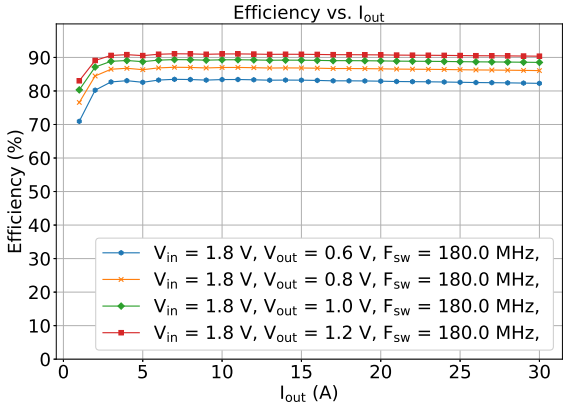

Figure 1: Efficiency vs I_{OUT} for V_{IN}=1.8V.

4 General Description

The Fe1508, Power System on a Chip (PwrSoC), is an 12-phase interleaved buck converter with fully integrated powertrain, including thin-film ferromagnetic power inductors. The Fe1508 integrates digital interface, power management, voltage control and powertrain circuitry (including power FETs, inductors and capacitors) all in one die. The Fe1508's precise voltage, fast transient, high bandwidth regulation, coupled with high switching frequency powertrain driving Ferric's magnetic composite integrated inductor technology, deliver high efficiency, high-quality power in a small footprint and volume to reduce board area, layout complexity, and Bill of Material (BOM).

5 Typical Package Footprint

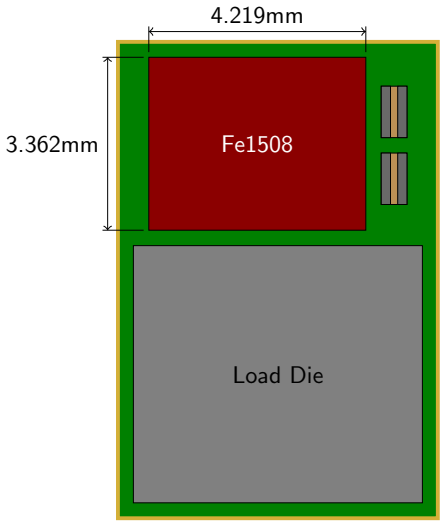

Figure 2: Typical package footprint.

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7 Electrical Specifications

In Table 1, V_{IN} = AVDD18 = VDDIO = 1.8V, V_{OUT}=0.9V, T_J=[-40,125]°C. Typical values are at T_J=25°C.

Table 1: Electrical specifications.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN Voltage Range	V_{IN}	AVDD18 $\geq$ V_IN	1.6	1.8	2.0	V
Output Voltage Range	V_{OUT}	$V_{IN}\geq$ 1.8V	0.25		1.4	V
Output Voltage Resolution	$V_{OUT,RES}$			1.7		mV
Steady State Output Current	I_{OUT}				20	A
Number of Powertrain Phases	N_{PHASES}		2		12	Phases
DC Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT\_Line}}$			$\pm$ 0.5		%
DC Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT\_Load}}$			$\pm$ 0.5		%
Output Voltage Ripple	ΔV_{RIPPLE}	$C_{LOAD}\geq$600nF		1		mV
Switching Frequency	f_{SW}		100	180	200	MHz
Load Current Step Up Response	$\lvert\Delta V_{OUT,UP}\rvert$	ΔI : 8A to 23A Δ t = 2ns C_{LOAD}=600nF		80		mV
Load Current Step Down Response	$\lvert\Delta V_{OUT,DN}\rvert$	ΔI : 23A to 8A Δ t = 2ns C_{LOAD}=600nF		80		mV

8 Application Schematic

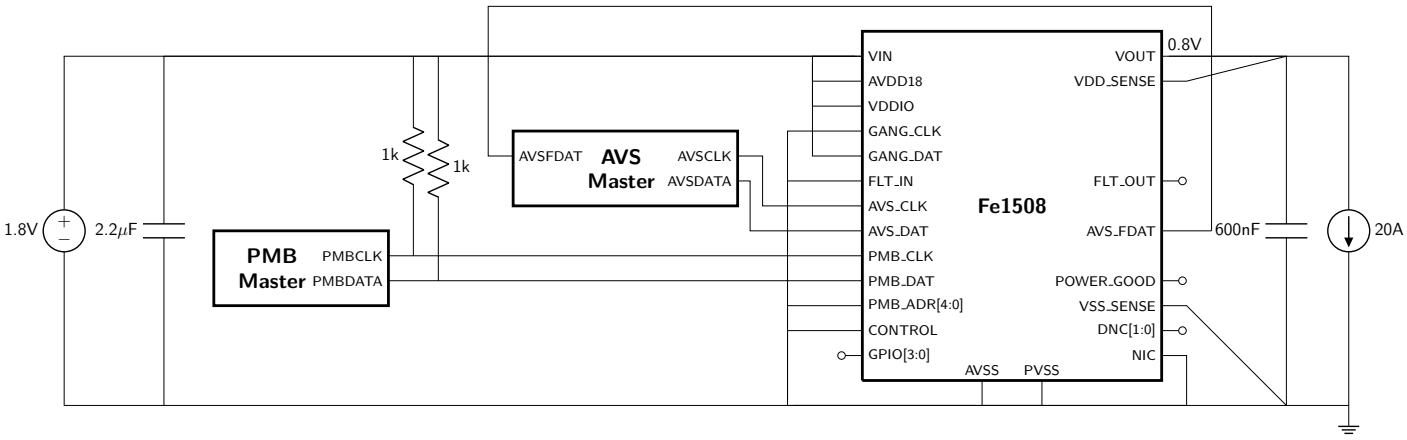

Figure 3: Application schematic for single chip operation with both PMBus and AVSBus Interfaces.

3A, Multiphase, Chip Scale DC-DC Step-Down Power Converter with Integrated Inductors and Digital Power Interface

1 Features

- 8 phase buck converter with fully integrated power switches and thin film ferromagnetic power inductors
- Efficiency >80%
- Input Voltage Range: 1.8V - 2.5V
- Output Voltage Range: 0.6V - 1.5V
- High Switching Frequency: 50-100MHz
- Wide Loop Bandwidth: Up to 10MHz
- Output Voltage Ripple: <10mVp-p at full load
- True Point-of-Load (PoL) Sensing
- Output Low Dropout Linear Regulator (OLDO)
- 1MHz PMBus-Compliant Serial Interface
- Gang Operation
- Automatic Phase Shedding
- Input Voltage, Output Voltage, Output Current and Temperature Telemetry
- OVP, OTP, UVLO, OCP Fault Responses
- 7.8mm^2 footprint

2 Applications

- Point of Load regulation for processors, DSPs, FPGAs and ASICs
- Noise sensitive applications such as A/V, RF and Gbit I/O
- Embedded computing, Blade servers, RAID storage systems, LAN/SAN Adapter Cards, Wireless Base Stations, Industrial Automation

3 Performance

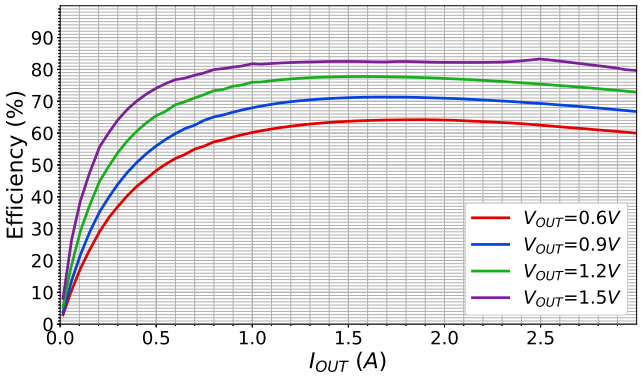

Figure 1: Efficiency vs I_{OUT} for V_{IN}=1.8V.

4 General Description

The FE1038E, Power System on a Chip (PwrSoC), is an 8-phase interleaved Buck converter with fully integrated powertrain, including thin-film power inductors. The Fe1038 integrates digital interface, power management, voltage control and power train circuitry (including power FETs, inductors and capacitors) all in one die, 2.24mm x 3.49mm. The Fe1038's precise voltage, fast transient response, high-bandwidth regulation, coupled with high switching frequency powertrain driving magnetic composite integrated inductor technology, delivers high efficiency, high-quality power in small footprint to reduce board area, layout complexity, and Bill of Material(BOM).

5 Typical Package Footprint

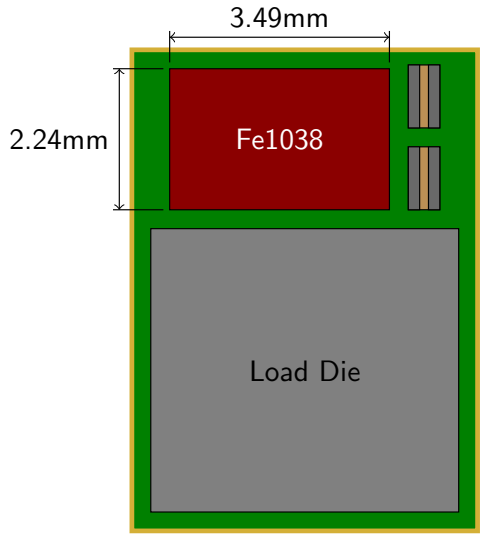

Figure 2: Typical package footprint.

6 Contact Information

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7 Electrical Specifications

In Table 1, V_{IN} = AVIN = VDDIO = 1.8V, V_{OUT}=1.2V, T_J=[-40,125]°C. Typical values are at T_J=25°C.

Table 1: Electrical specifications.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN Voltage Range	V_{IN}		1.8		2.5	V
Output Voltage Range	V_{OUT}		0.6		1.5	V
Output Voltage Resolution	$V_{OUT,RES}$			0.8		mV
Output Voltage Accuracy	$V_{OUT,ACC}$			±1.0		%
Steady State Output Current	I_{OUT}				3	A
Number of Powertrain Phases	N_{PHASES}		2		8	Phase
DC Line Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Line}$	Iout = 0A, 1.8V≤V_{IN}≤2.5V		± 0.5		%
DC Load Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Load}$	I_{out} = 0A to 3A		± 0.5		%
Output Voltage Ripple	ΔV_{RIPPLE}	C_{LOAD}≥1μF		10		mV $_{p-p}$
Switching Frequency	f_{SW}		60	90	120	MHz
Load Current Step Up Response	$\lvert\Delta V_{OUT,\ UP}\rvert$	Δ I_{OUT} : 1A to 2A, Δ t = 200ns		15		mV $_{p-p}$
Load Current Step Down Response	$\lvert\Delta V_{OUT,\ DOWN}\rvert$	Δ I_{OUT} : 2A to 1A, Δ t = 200ns		15		mV $_{p-p}$

8 Typical Application Diagram

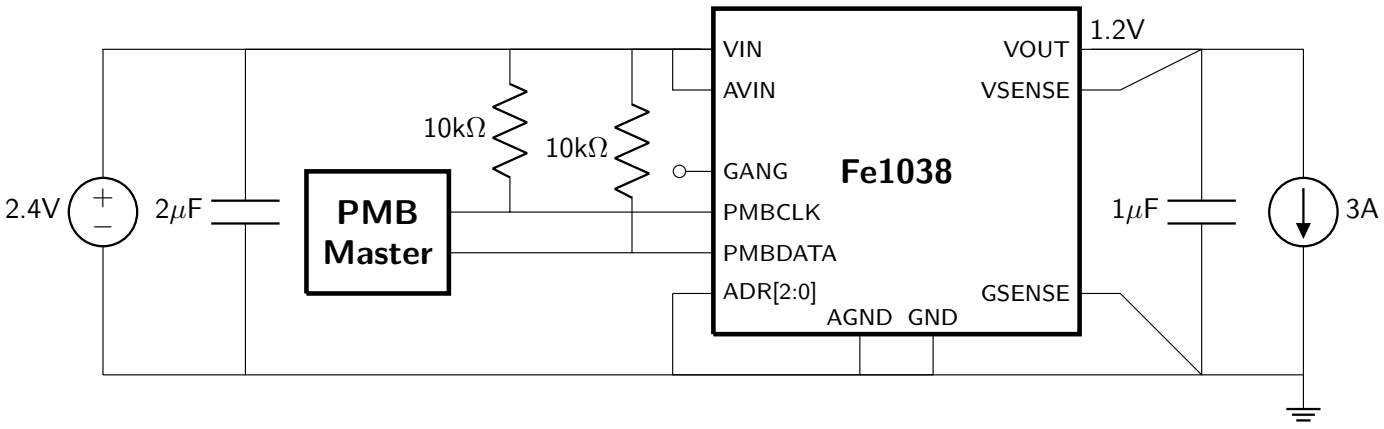

Figure 3: Typical application schematic