Arteris IP

COMPANY OVERVIEW FOR HOTCHIPS 2021

KURT SHULER
VP of Marketing

Arteris IP – The Leading SoC Integration IP Company

FOUNDED IN 2003, HEADQUARTERS IN SILICON VALLEY

Data is current as of July 16, 2021

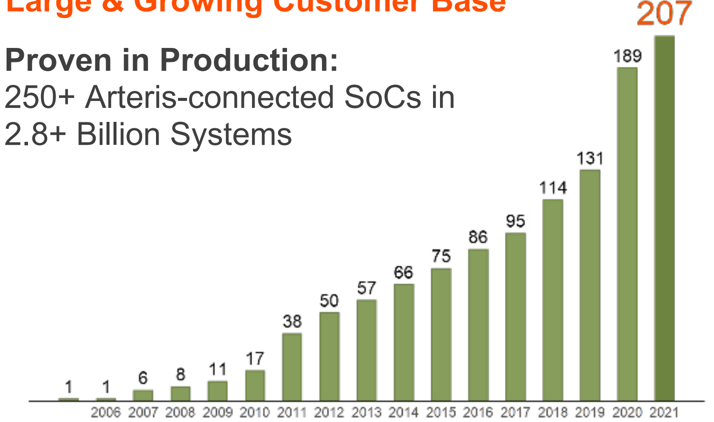
Continuous Technology Innovation

FlexNoC®	2010	Main interconnect, 2nd gen
FlexWay™	2010	IP subsystem interconnect
FlexPSI	2013	All-digital interchip link
FlexNoC Resilience	2014	Resilience for ISO 26262
FlexNoC Physical™	2015	Links to physical SP&R
Ncore®	2016	Cache coherent interconnect
PIANO®	2017	Automated timing closure
CodaCache®	2018	Independent last level cache
AI Package™	2019	Machine learning interconnect
Ncore 3	2020	CHI & ACE cache coherency

Global Presence

Large & Growing Customer Base

Proven in Production:
250+ Arteris-connected SoCs in
2.8+ Billion Systems



Top Semis use Arteris IP

Publicly Disclosed Customers

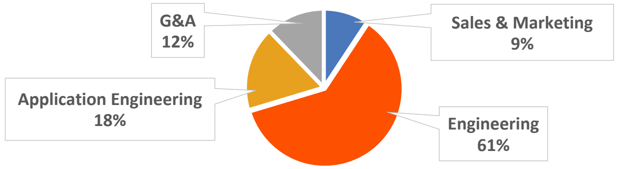
SAMSUNG, mobileye, BOSCH, Baidu 百度, NXP, ALTERA, UNISOC, Movidius, Toshiba, SiFive, socionext, ST, Texas Instruments, ULTICHIP, arbe, RENESAS, HAILO, Achronix, flexlogix, MegaChips, Horizon Robotics, KYOCERA, Hisense, pixelworks, BlueOcean, Schneider Electric, GCT, nextchip, octasic, SEQUANS, VeriSilicon, MONTAGE Technology, SEMIDRIVE, Autotalks, AMPERE, Lynxi, Canaan, 国民技术, MORNINGCORE, AutoChips, Iluvatar CoreX, CALTERAH, Enflame, BITMAIN, BLACK SESAME, picocom, Silicon Mobility, Cambricon, 東京大学, UHNDER, siengine, VITEC, SiMa.ai, NETINT, Synaptics, Corerain, ESWIN, nuvoTon, RECOGNI, GOKE, indie, T-HEAD, METAX, MAXLINEAR, ANALOG INFERENCE, INNOSILICON, INUITIVE

In Leading Systems

Connected by Arteris Ecosystem

arm, SYNOPSYS, tsmc, SAMSUNG, cadence, ISO 26262, exida, RESILTECH, CXL Compute Express Link, CCIX

Interconnect Technology Think Tank



Arteris IP Management Team

Charlie Janac
Chairman, President & CEO

David Mertens
VP, Worldwide Sales

Laurent Moll
Chief Operating Officer

Kurt Shuler
VP, Marketing

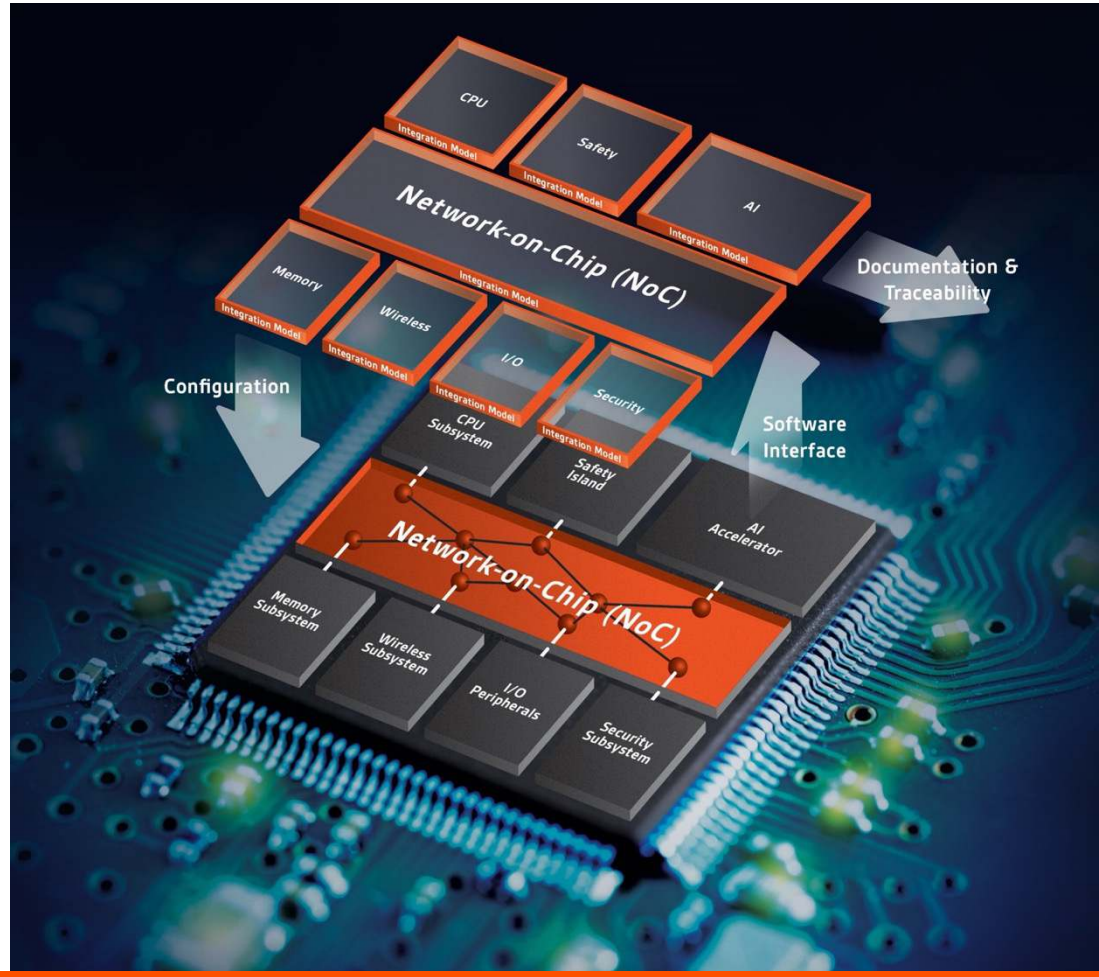
Nick Hawkins
Chief Financial Officer

Paul Alpern
VP & General Counsel

Isabelle Geday
VP & General Manager IPD

SoC is Composed of Internal & Commercial IP Blocks

- During **Specification & Integration**, the SoC is a virtual object described in XML, using the IP-XACT standard
  - Accelerates IP deployment
  - Automates documentation & traceability
  - Whole solution → IP assembly methodology
- During **Architecture & NoC RTL Assembly**, IP blocks are best connected by Network-on-Chip (NoC) Interconnect
  - NoCs connect all major IPs on SoCs
  - NoCs carry all interesting data traffic
  - NoCs are the most configurable of all IPs

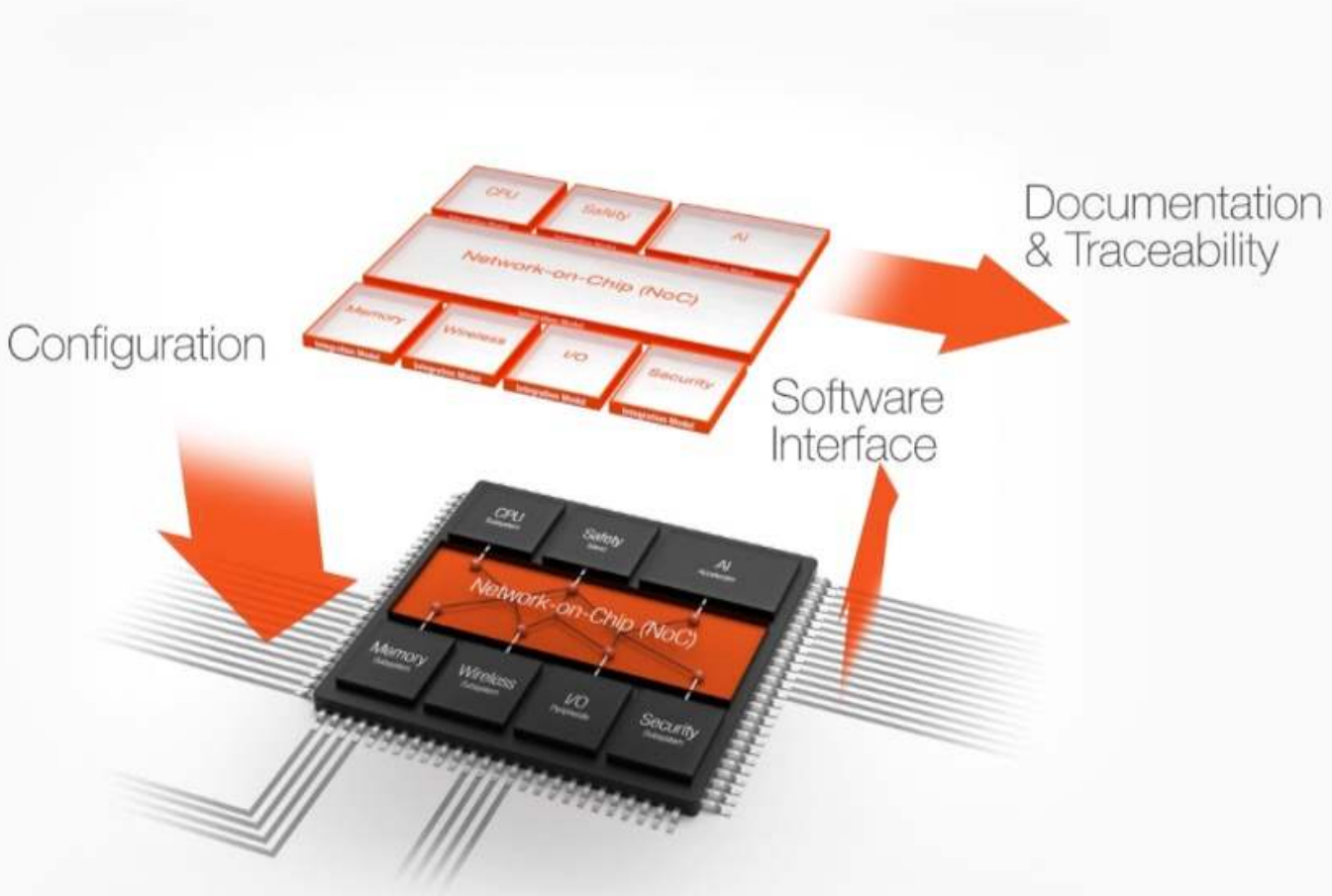


Arteris IP Enables Customers to Deploy & Connect Semiconductor IP to Make Better SoCs

NoC Interconnect IP + IP Deployment = SoC System IP

- Arteris IP acquired Magillem Design Services assets in November 2020
- Combined company is the world's largest SoC Integration company
  - NoC Interconnect IP (Arteris IP)
  - IP Deployment Technology (former Magillem)
- 206 employees in 7 countries
- Headquarters in Silicon Valley

Arteris IP NoC IP & IP Deployment Technology Integration



IP Packaging with IP-XACT

SoC Platform Creation

SoC Assembly

NoC Topology Synthesis

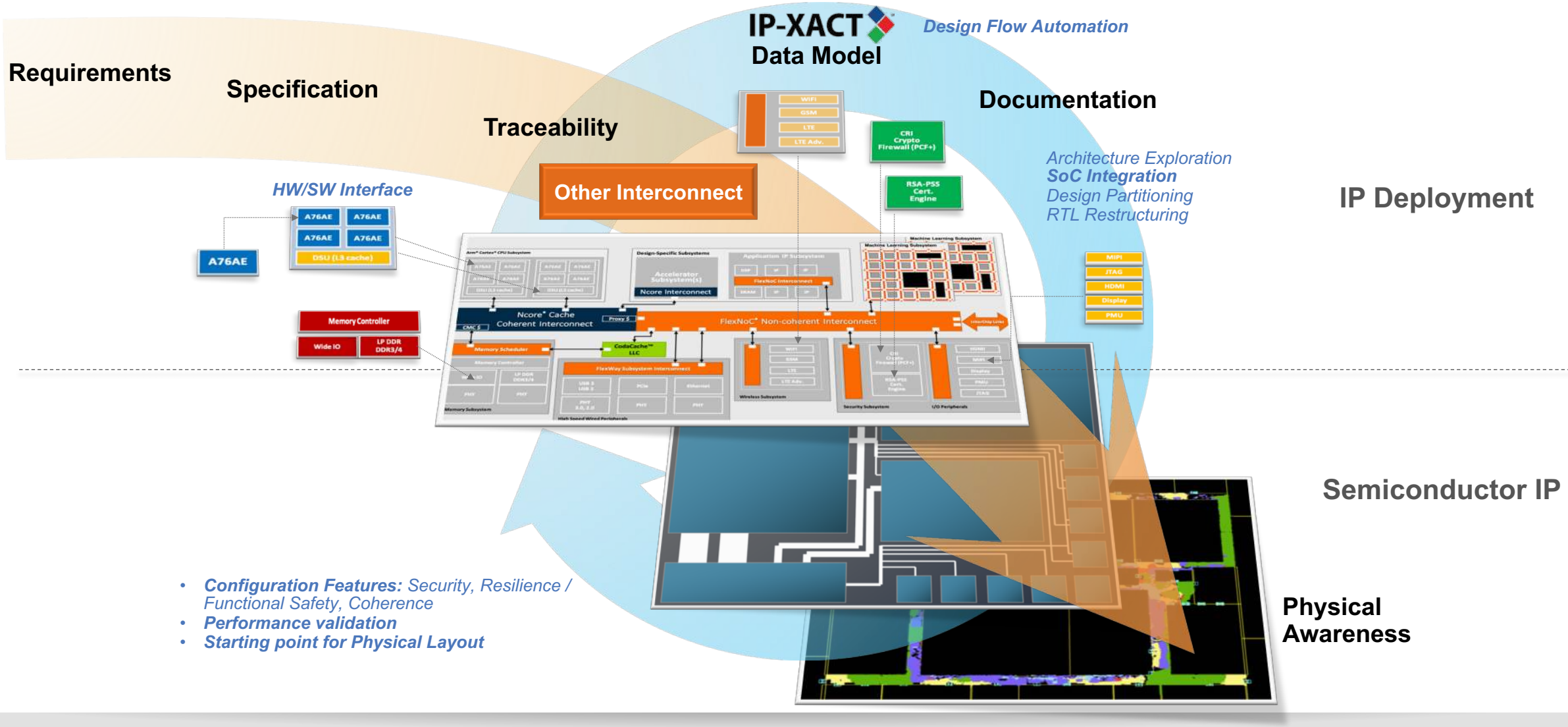
NoC Optimization

Memory Map Management

Embedded Software Support

Collateral Generation

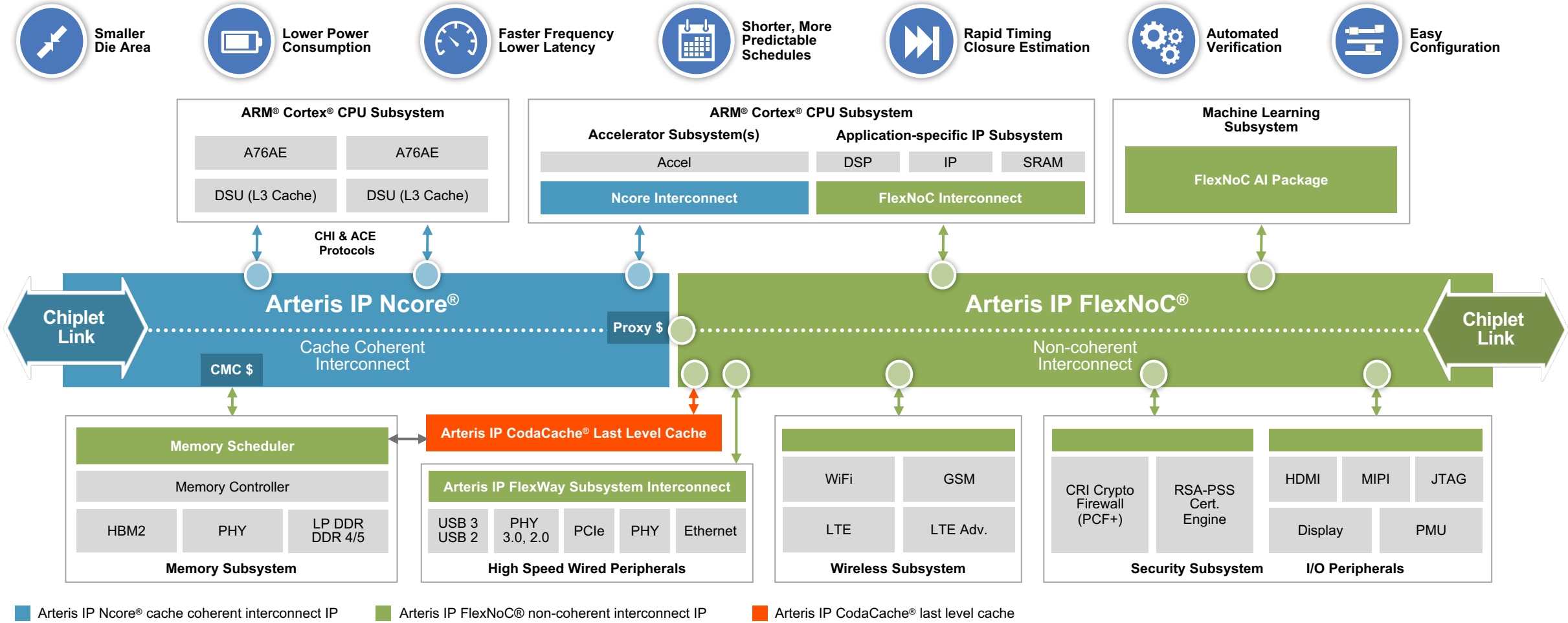
Arteris IP Deployment Software & Arteris Semiconductor IP Synergy



- ***Configuration Features:*** *Security, Resilience / Functional Safety, Coherence*
- ***Performance validation***
- ***Starting point for Physical Layout***

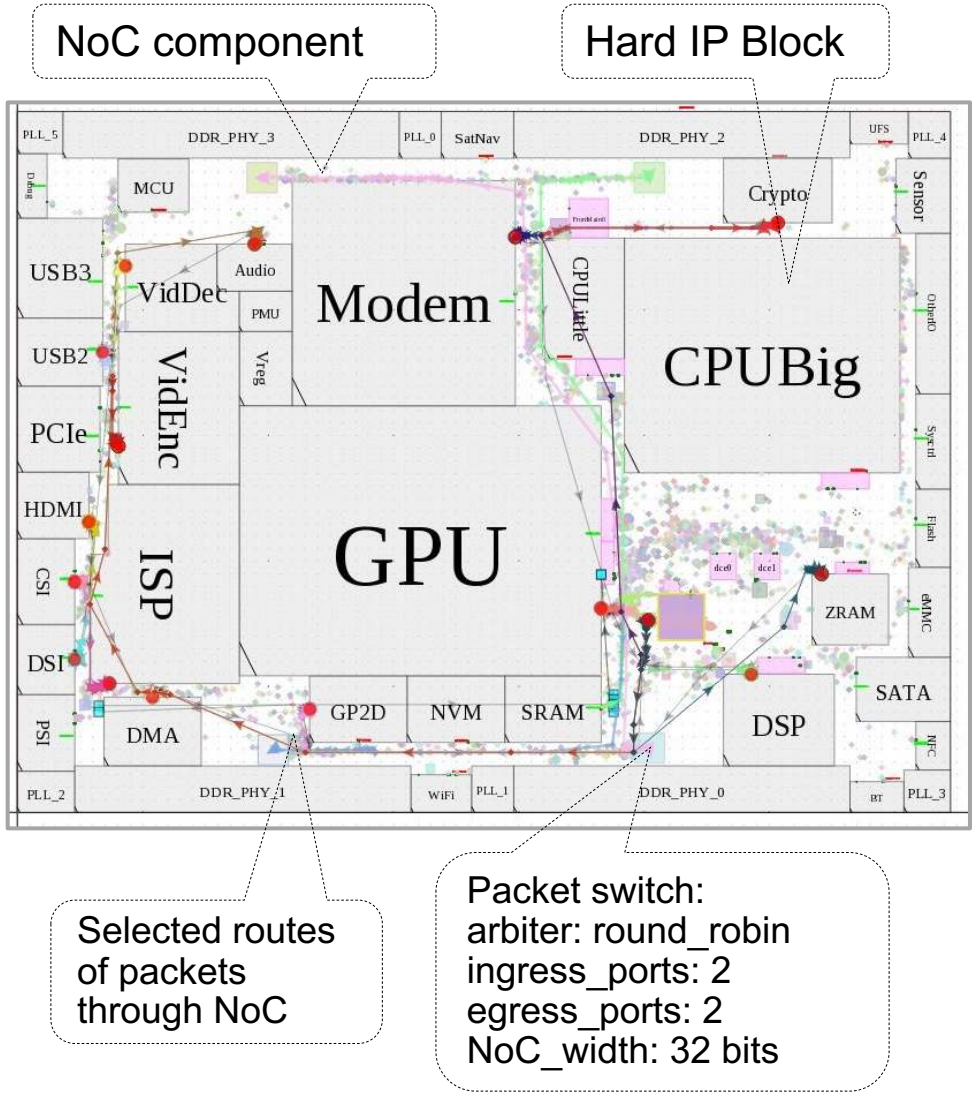
Using Networking Techniques for Improved On-Chip Communication & Data Flow

INTERCONNECT IP IS CRITICAL TO EVERY SOC TO ENABLE NEXT-GENERATION TECHNOLOGIES



NoC Interconnect IP Implementation

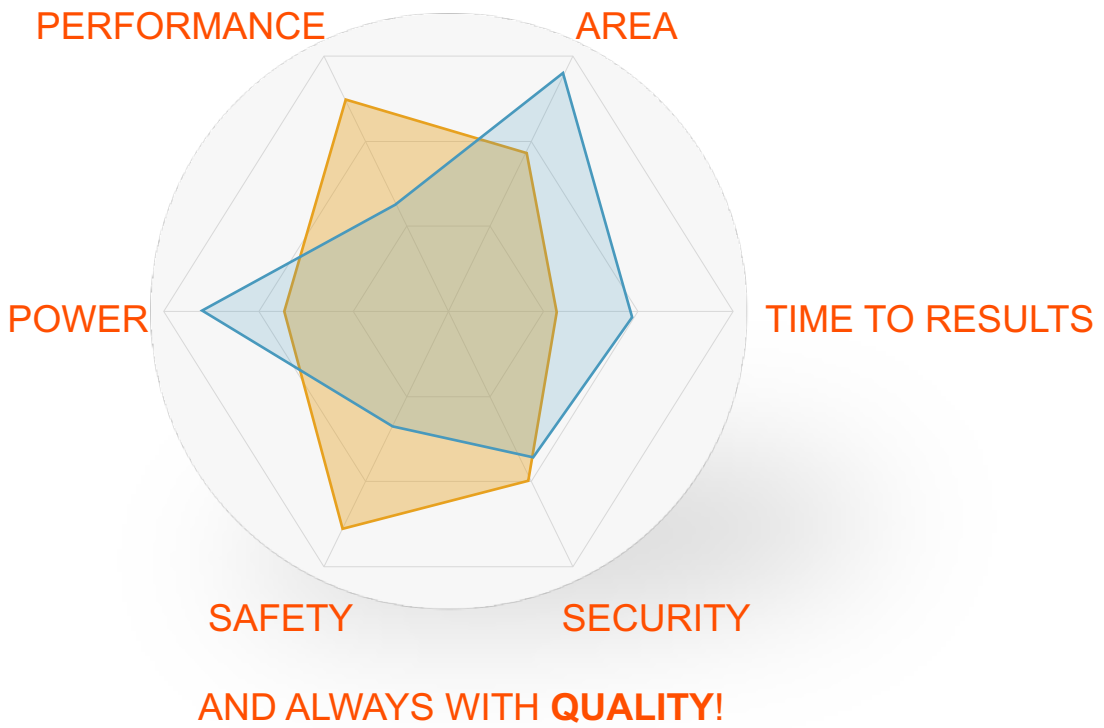
- NoC IPs are built of protocol converters, packetizers, switches, adapters.
  - NoC IPs fill area between hard IPs at both SoC Top-Level & inside SoC sub-systems
- NoC creation tools treat components as multi-variant parametrized abstractions
  - Generated Verilog RTL depends on parameter values
- Enables optimization between architectural specs (latency, QoS), power consumption and physical constraints



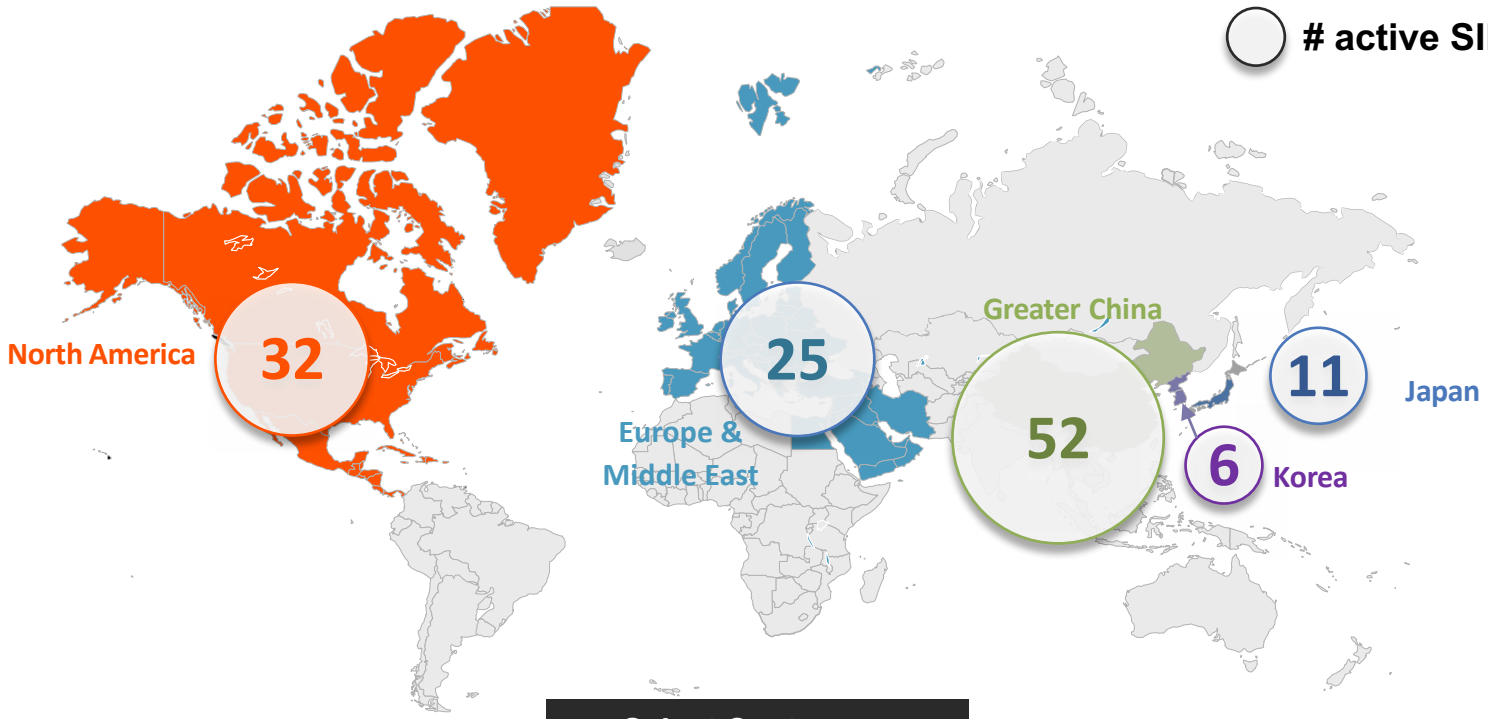
Arteris IP Network-on-Chip Supports Advanced Architectures

LOWERING R&D & UNIT COSTS THROUGH ADVANCED FEATURES, AUTOMATION & LEADING PPA

- **Performance:** Up to 2Ghz frequency @16nm, >2TBit/sec bandwidth with 1024-bit links
- **Power:** <0.5mW idle power/1M gates@16nm, 0-cycle unit-level wake up, 3-level clock gating
- **Area:** Endpoint NoC = Lower area/Interconnect function (typically 25+% lower than hybrid buses or corner router NoCs)
- **Time to Results:** Design exploration, multi-level modeling, auto test bench generation, physical awareness, design flexibility, 3-day NoC for complex SoC derivatives
- **Safety:** Resilience – ISO 26262 ASIL B-D capable, Functionally safe domains
- **Security:** Customer extensible firewalls and access controls



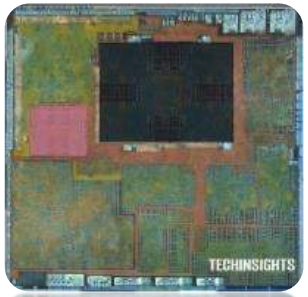
Globally Diversified Customer Base

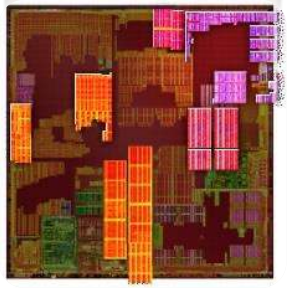


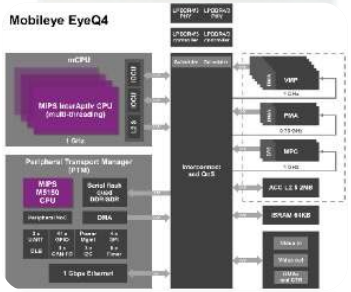
Select Customers

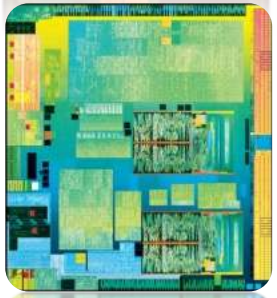
arbe · Autotalks · Baidu 百度 · BOSCH · Enflame 燧原科技 · ST life.augmented · KYOCERA · nuvoTon · mobileye An Intel Company · NXP · RENESAS · SAMSUNG · SEQUANS · SiFive · Texas Instruments · T-HEAD

Proven Product Quality Shipping 250+ Connected SoCs in 2.8+ Billion Systems Across 165+ Customers





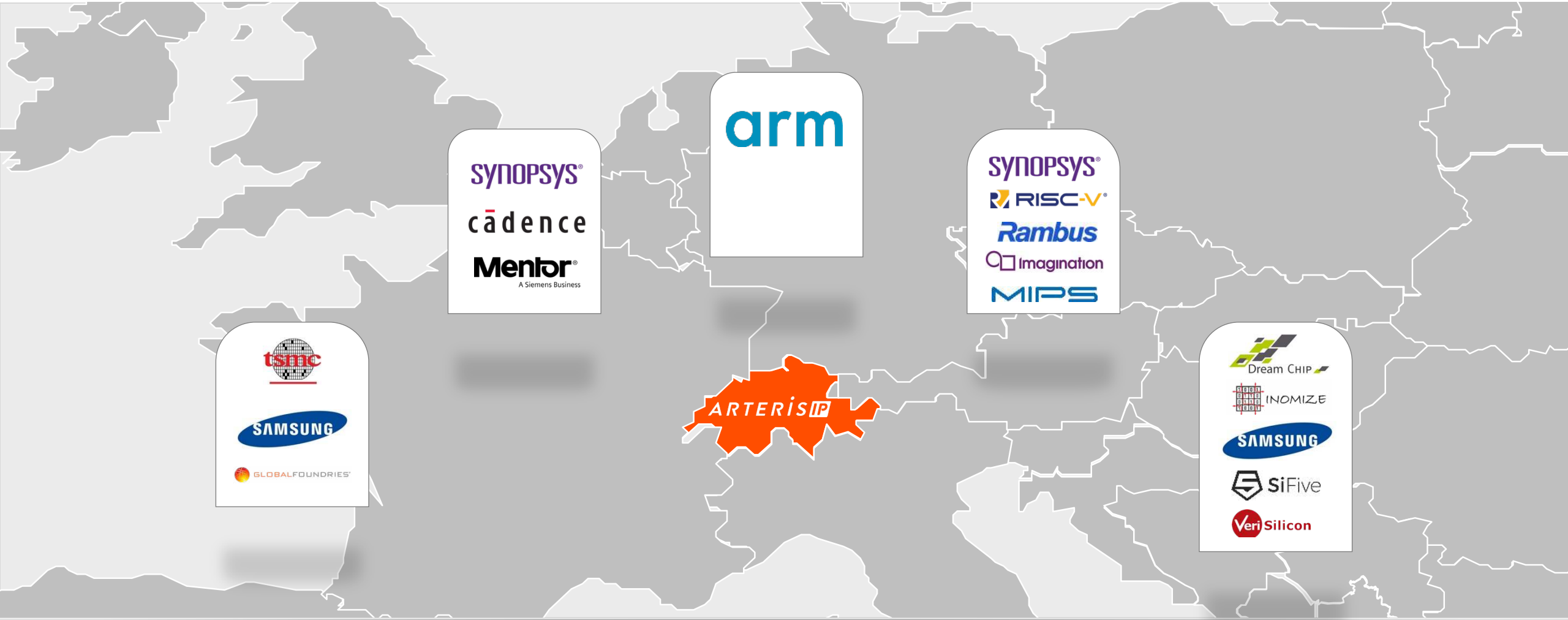




PROVEN IN PRODUCTION!

Arteris IP Ecosystem → Be the Switzerland of IP

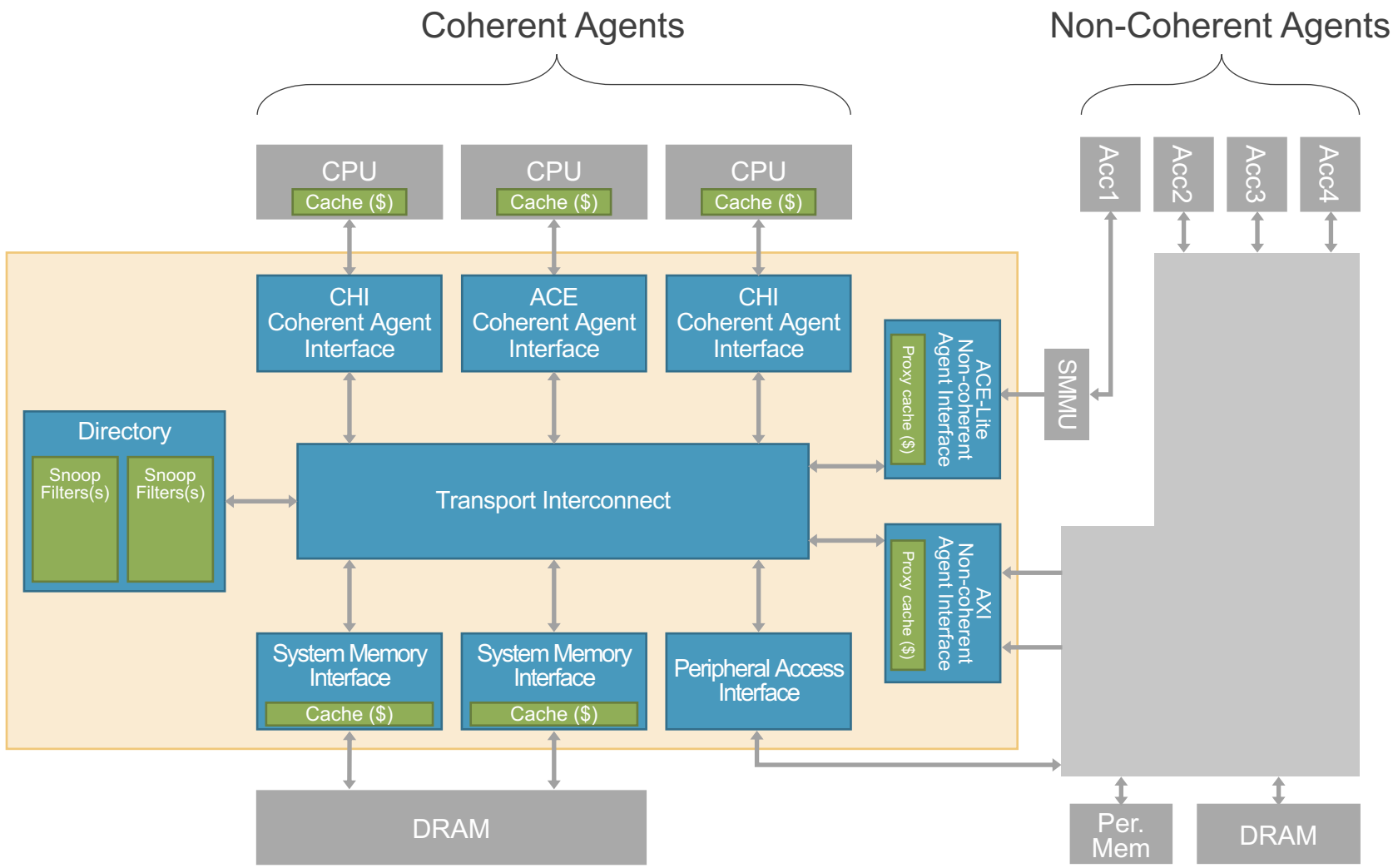
TRUSTED, NEUTRAL PARTNER FOR ALL IP PROVIDERS AND SEMICONDUCTOR MAKERS



Semiconductor IP Products and Technology

- Proven NoC technology used in billions of SoCs
- 1-2 new products per year addressing SoC innovation
- 4-6 enhancement releases per year for customer feature delivery
- Mature quality processes for trouble free deployment
- Enabling SoCs with greater performance at lower cost(s) on predictable schedule

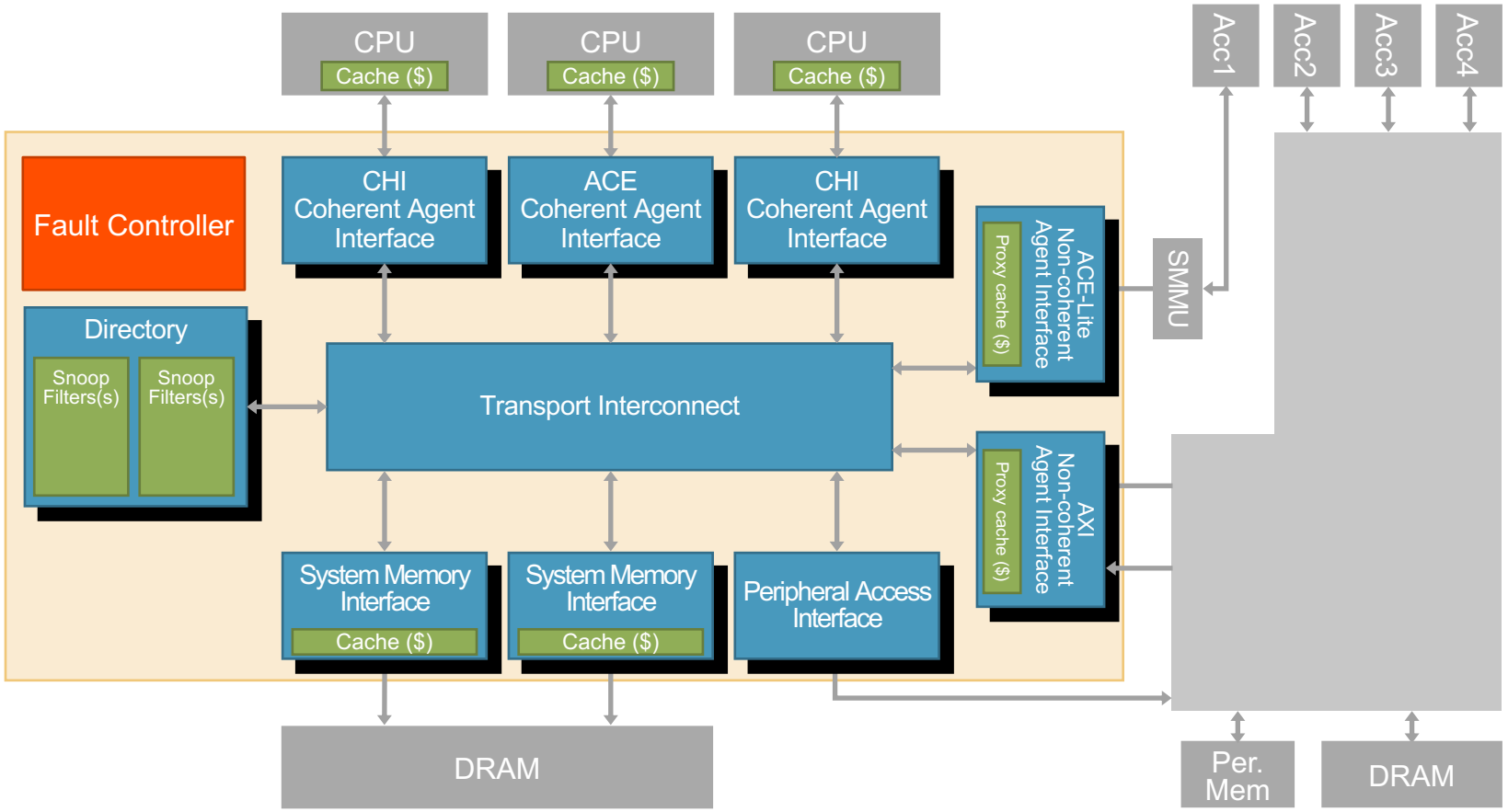
Ncore® Cache Coherent Interconnect



Ncore Features

- Multi-Protocol Coherency
  - CHI-A, CHI-B
  - ACE
  - ACE-Lite, ACE-Lite-E
  - AXI
- Multiple Networks
- Multiple Cache Options
- Connectivity
  - Up to 64 coherent Ports
  - Up to 64 IO coherent Ports
  - Up to 16 Memory Ports
  - Up to 16 Peripheral Ports
  - Up to 16 Directory Ports
- Multiple Clock/Power Domains
- 1.6 GHz in 16 FFC
- Resilience Option

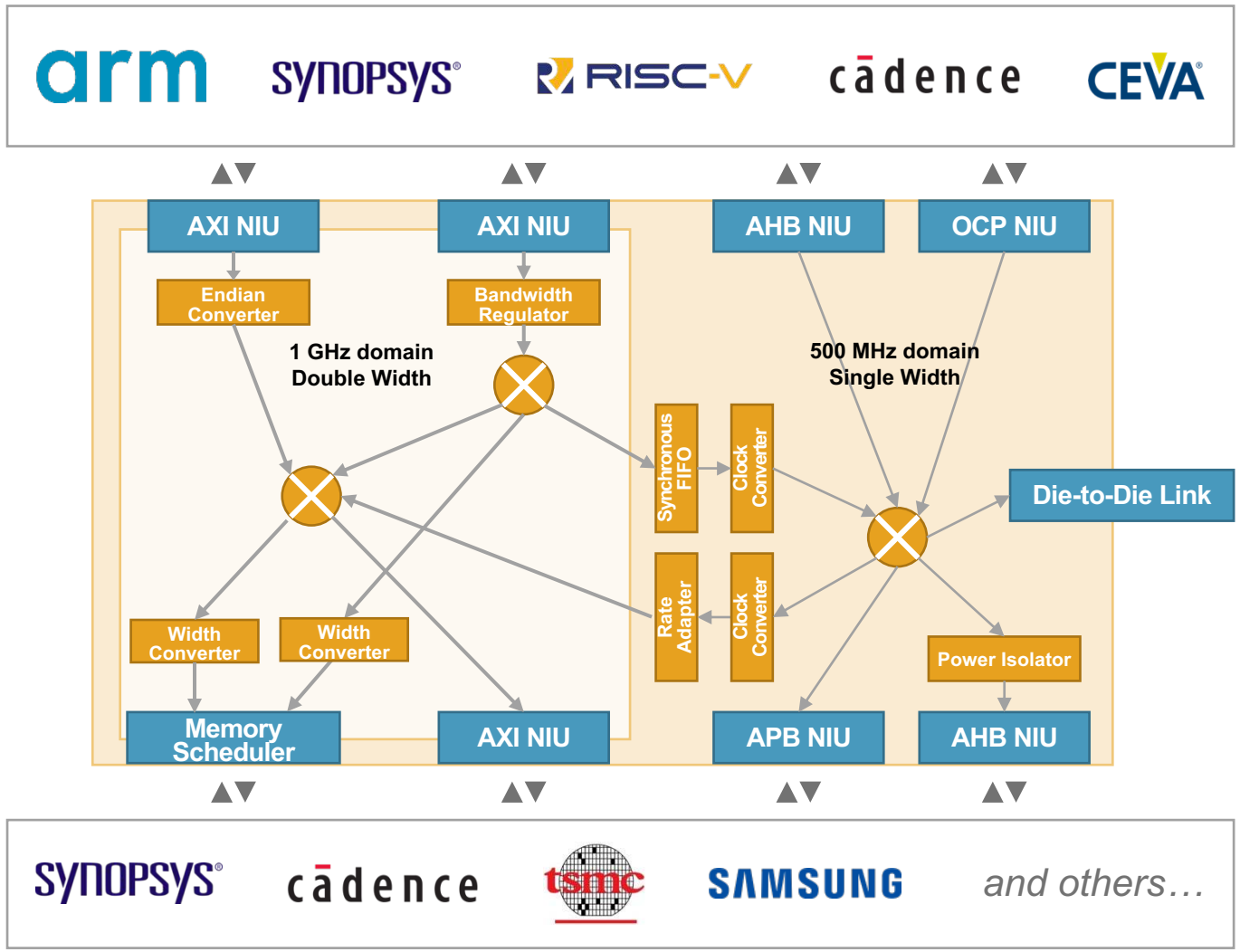
Ncore® Resilience Package



Functional Safety Capabilities

- Supports multiple Clock/Voltage/Power domains
- Minimized hardware duplication
  - SRAMs are shared
- Transport is ECC protected
- Placeholders for ECC protection at boundaries
- Integrated Fault Controller
- Up to ISO 26262 ASIL D
  - SPFM > 99%, LFM > 90%
  - FMEDA for a reference configuration provided by Arteris IP
- Working with ResilTech on analysis
- exida ISO 26262 assessment starts Jan 2021

FlexNoC® Non-Coherent Interconnect features

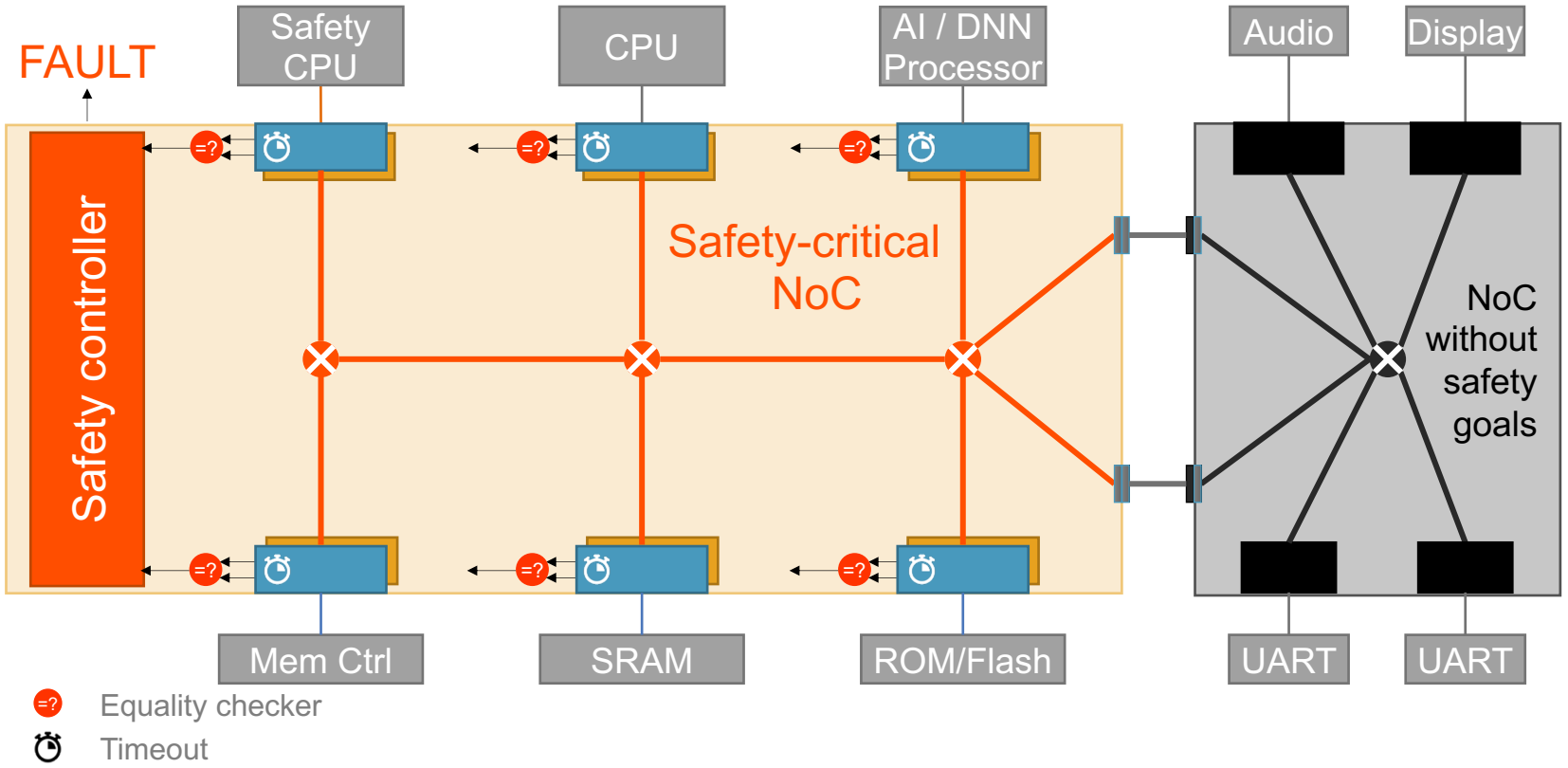


*NIU = "Network Interface Unit"

Network-on-Chip Technology

- Network Interfaces
  - ACE-Lite, AXI, AHB, APB, OCP, PIF
- Transport
  - Switches, FIFOs, Converters, VC-Links, source-synchronous async bridges, broadcast/multicast
  - Any topology
- Quality of Service (QoS)
  - Bandwidth Regulator & Limiter
- Domains
  - Multiple Clock, Power & Voltage Domain Support
- Power Management, unit level clock gating
- Security
  - Native & User Defined Firewall
- Memory Scheduler/Interleaver
- Safety – up to ISO 26262 ASIL D
- In-Silicon Debug
  - On-Chip Performance Monitoring and Debug

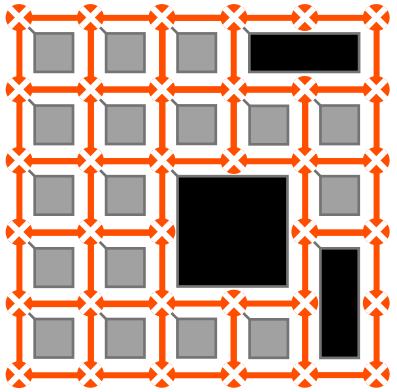
FlexNoC® Resilience – ASIL D Ready



- Unit duplication - fault detection
- ECC at interface & in-transport
- Packet consistency checkers
- Safety controller
- Fault reporting logic BIST
- Multi ASIL support
- Arm® Cortex®-R5, R7, R52 CPU support
- ISO 26262 support documentation (DIA, Safety Manual, FMEDA)

FlexNoC® AI Package

FOR ACCELERATED DEVELOPMENT OF MACHINE LEARNING SOCS



Regular (AI) Topologies

- Automated Topology generation
- Customization of automated results
- Flexible router architecture

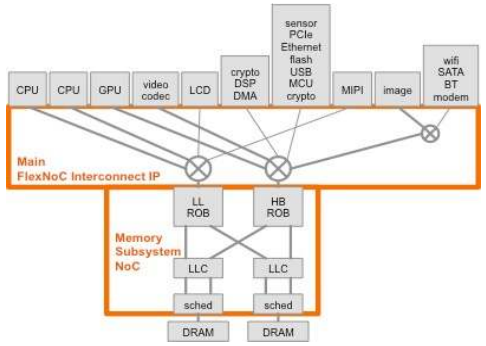
Huge Bandwidth

- Multicast
- Multi-channel HBM2 memory support
- High bandwidth datapaths

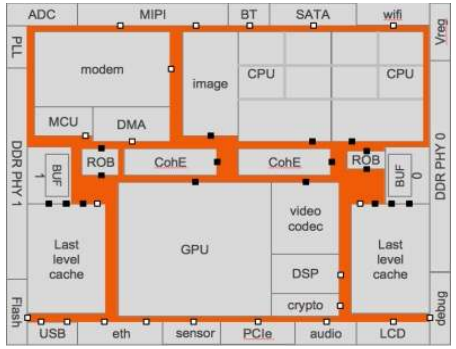
Large Chips

- Source synchronous communications
- VC-Links™ - Virtual Channels

PIANO® – Interconnect Timing Closure Estimation

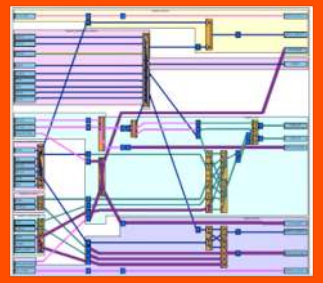


NoC Architecture



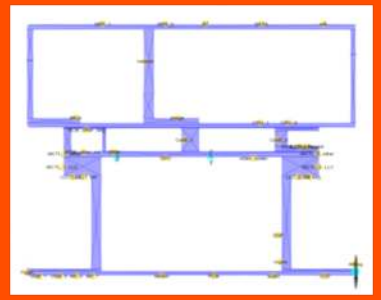
SoC Floorplan

Ncore / FlexNoC Logical IP



NoC topology

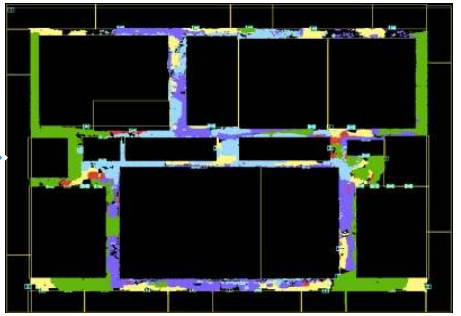
Ncore / FlexNoC Physical IP



Fast Iterations

PIANO

Pipeline configuration & placement

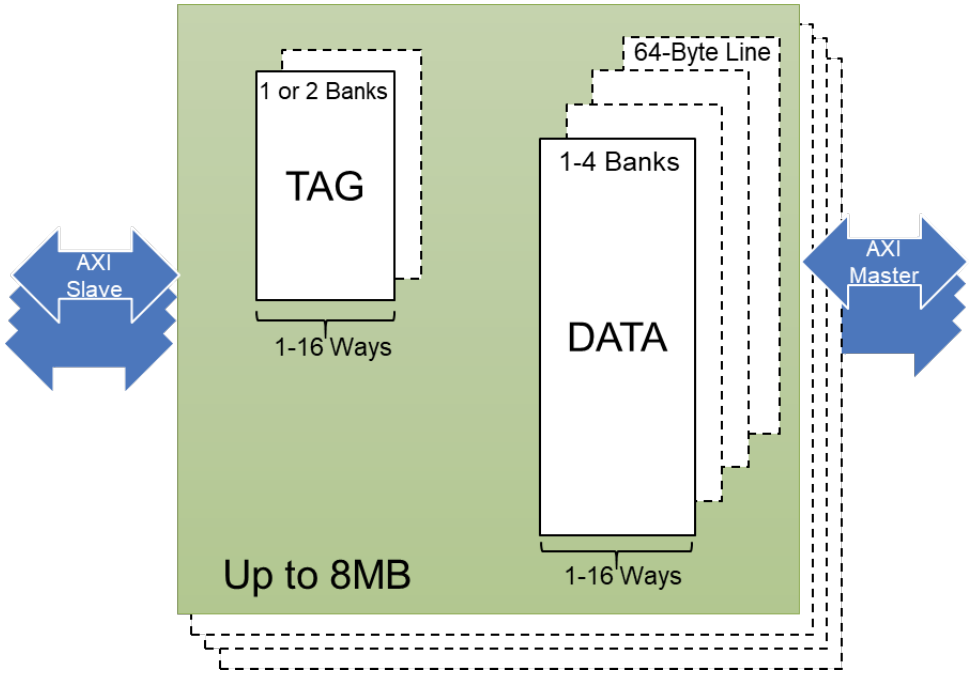


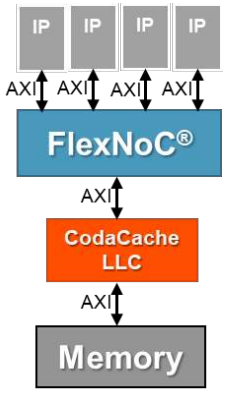
Physical Synthesis, P&R

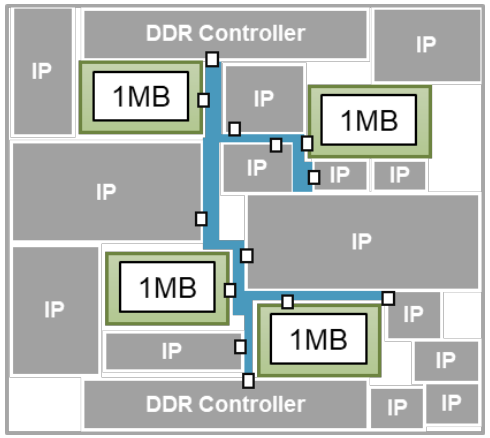
*Patents pending

CodaCache®

Standalone Last Level Cache







Major Features	
Master / Slave Interface	AXI4
Configuration Interface	APB
Data width	128/256-bit
Line Size	64 Byte
Cache Size	Up to 8MB per AXI Port
Associativity	1-16 ways
Frequency	Up to 1.2GHz 16FF+TT
Scratchpad Memory	Per-way configurable
Way Partitioning	
Assisted coherency management via hardware cache flush	

IP Deployment Software Solves SoC Integration Challenges

SOC IP BLOCKS HAVE HUNDREDS OF CONFIGURABLE KNOBS TO MANAGE

Missed scheduled deadlines

... due to lack of automation for and IP reuse strategy

Add automation to the design flow for higher productivity and better quality

Excessive SoC design re-spins

... due to errors caused by manual operations

Use industry standards for IP packaging, reuse and integration

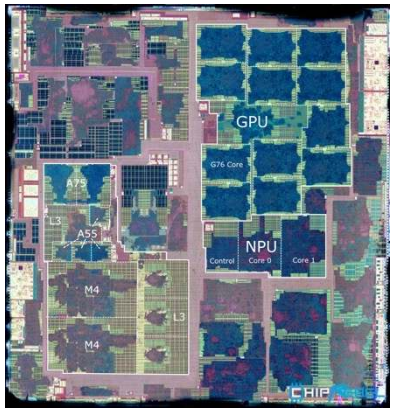
High cost of design (NPI)

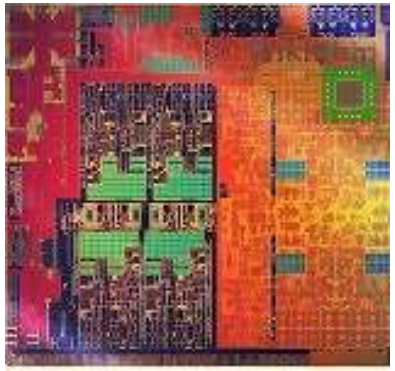
... due to inability to leverage resources, knowledge and IP

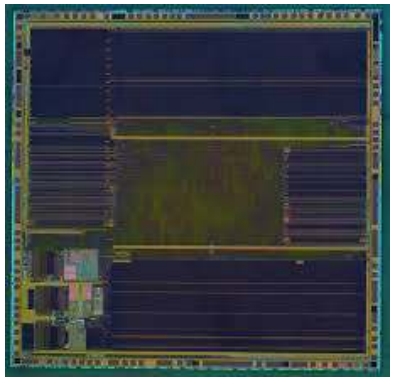
Increase efficiency through Content Management and turning data into an asset

Develop SoCs Faster with IP Deployment Technology

1. Deploy and reuse IP easily for **more predictable** SoC integration
2. Absorb **IP from different sources** with a unified methodology
3. **Interact with suppliers** and remote groups based on industry IP-XACT standard software
4. **Generate documentation** from design data – with Engineering Change Order (ECO) **traceability**







IP Deployment Solution

DEVELOP SOCS FASTER WITH IP DEPLOYMENT TECHNOLOGY & METHODOLOGY

Automate

Synchronize IP-XACT Standard

Configure

Fully Documented & Traceable Chip Design | Manage Register Configurations of IP Blocks | Assemble Multiple IP Blocks into SoC Devices | Link Design Parameters & Metadata

Architecture Requirements

Architecture Intent

Specification

Front-end Design Environment

Packaging Connectivity Registers CAD Flows

Design

Content Management

Content Publisher Link Tracer

Documentation

Real-time Analysis

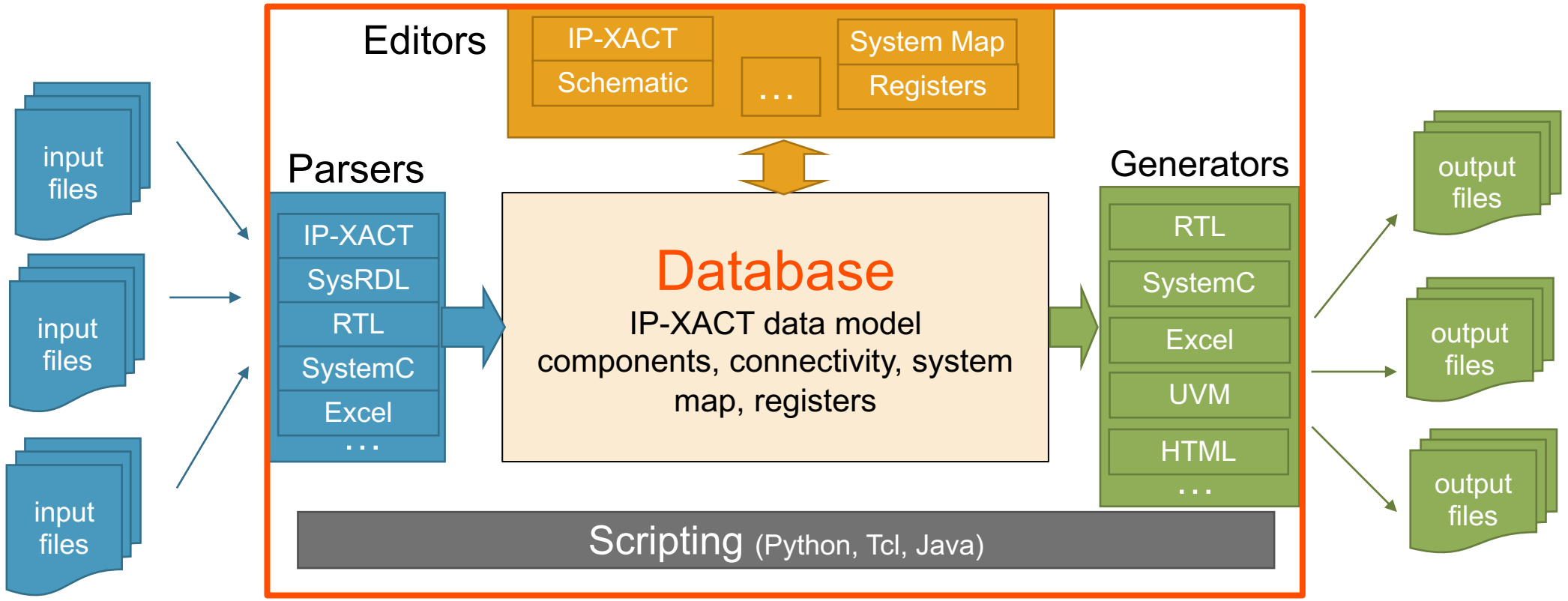
Dashboard / Search Focus Group

Design Intelligence

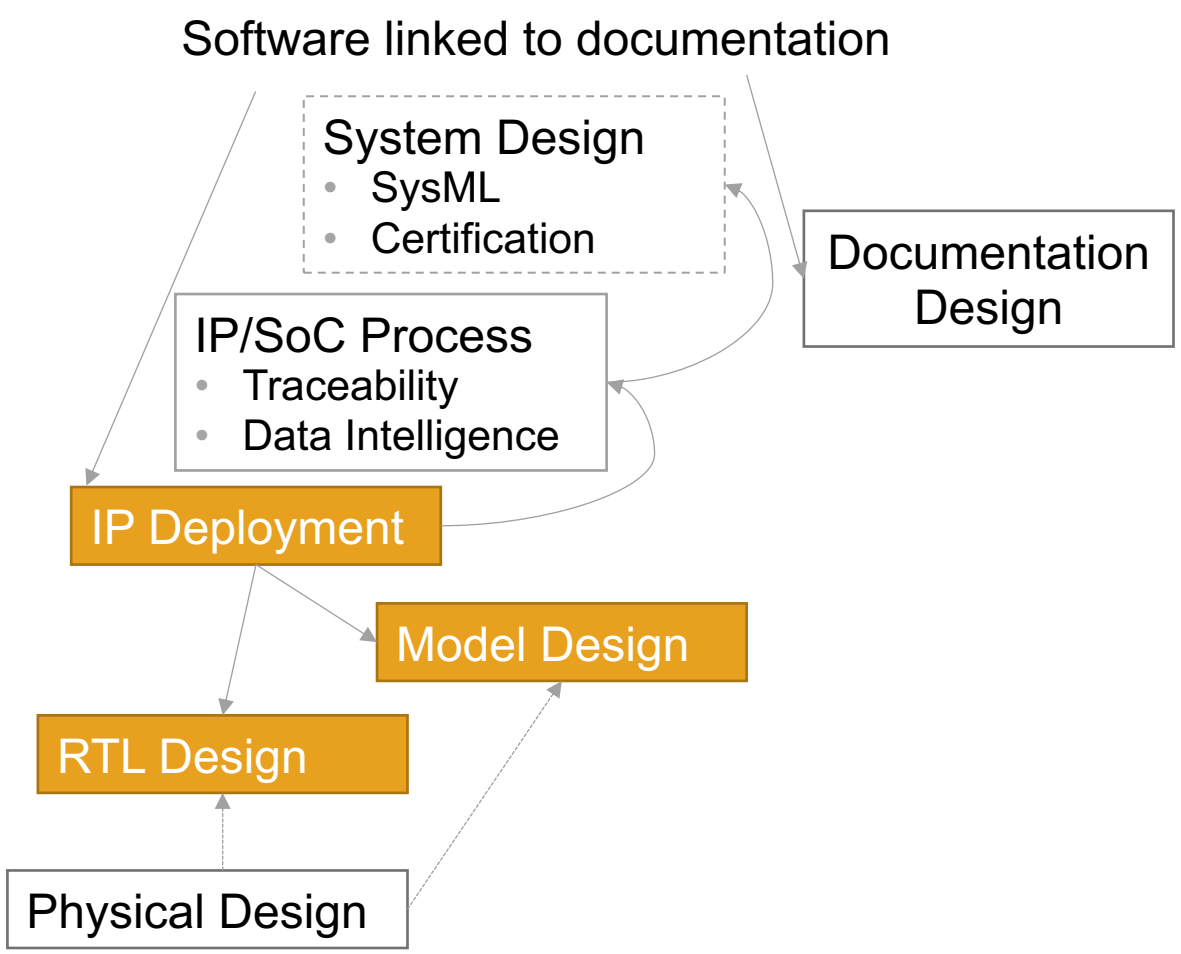
IP Deployment Software

Meet Project Deadlines | Improve Engineer Productivity | Eliminate Redundancies | Limit Costly Errors

SoC Integration Platform Overview



IP Deployment Software Stack to Accelerate SoC Delivery



Users:

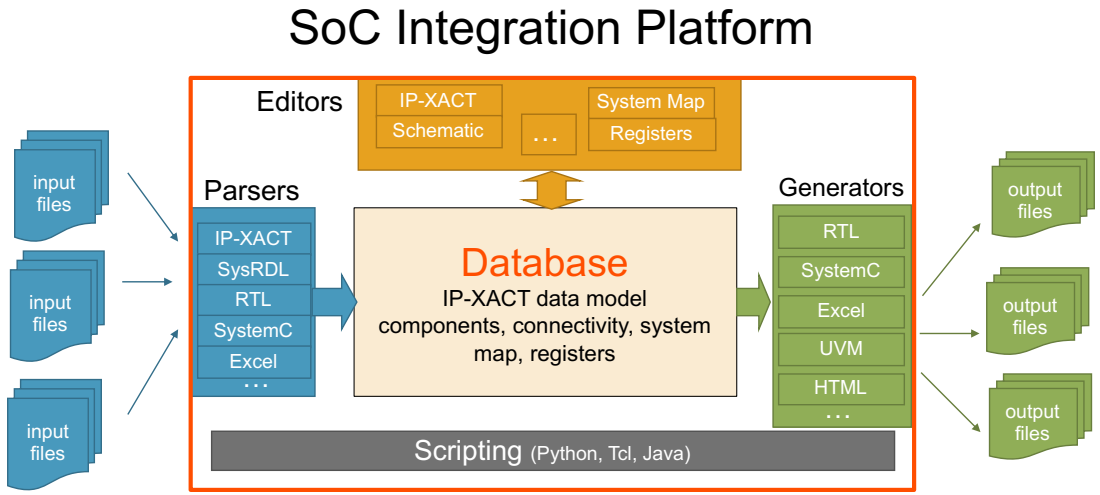
- Methodology director
- IP/SoC teams (HW, SW, verification)
- IP/SoC CAD team
- IP/SoC documentation team
- IP/SoC modeling team
- IP/SoC certification team
- System modeling team
- System certification team
- System documentation team

Applications:

- IP/SoC implementation
- IP/SoC HW/SW interface
- IP/SoC verification
- IP/SoC build flow
- IP/SoC modeling
- IP/SoC documentation
- IP/SoC certification
- IP/SoC portfolio
- System HW integration
- System certification integration
- Model-Based System Engineering (MBSE)

SW / Application independent

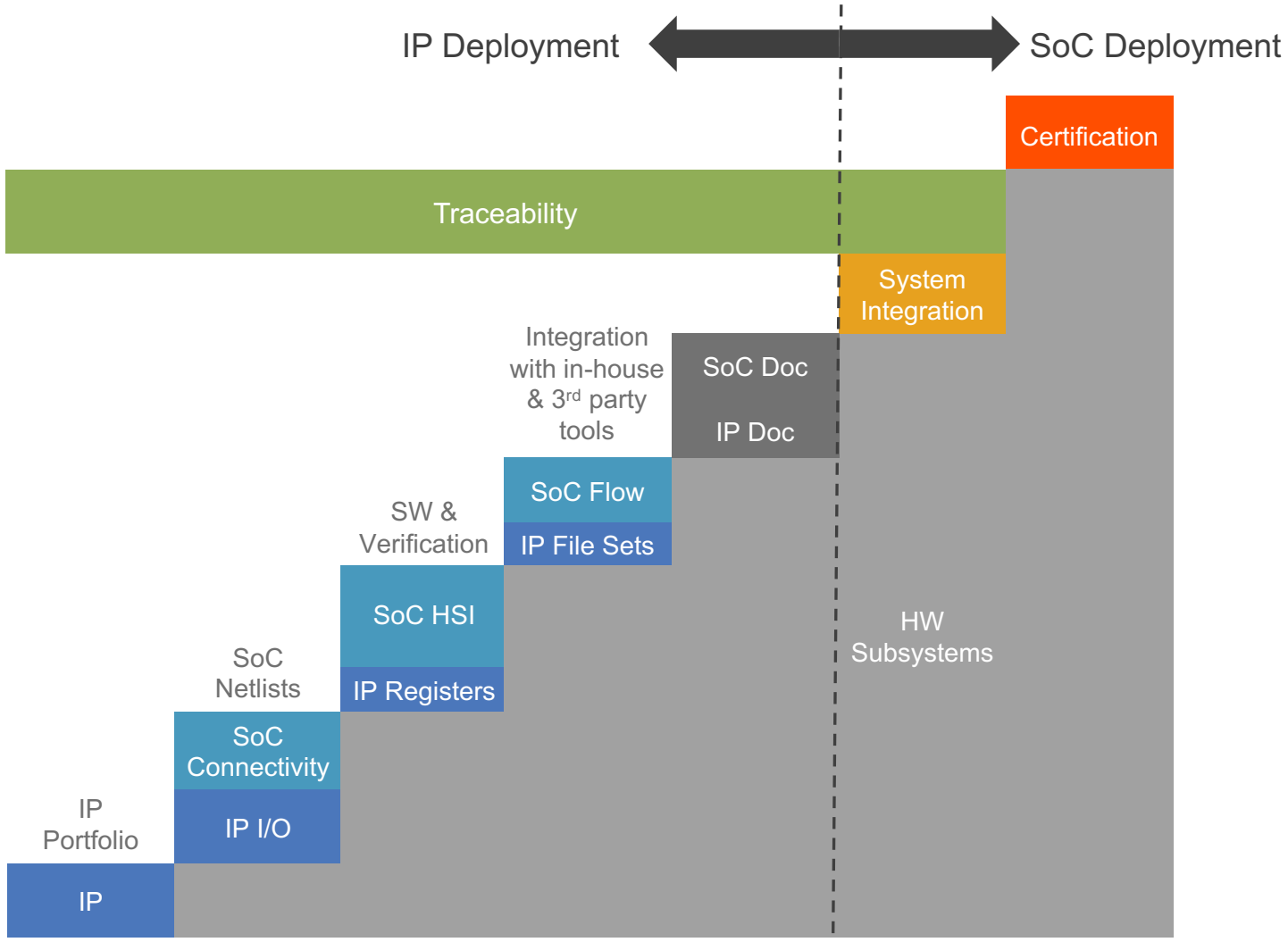
IP Deployment Product Line



together

Product	Main Function	Main Inputs	Main Outputs
MIP – packager	IP-XACT packaging	RTL, Excel	IP-XACT
MRE – SysRDL generator	SysRDL compiler	SystemRDL	IP-XACT
MRV – Register banks gen.	Register bank generation	IP-XACT, Excel	UVM / C / RTL
MPA – Assembly RTL	Platform assembly	IP-XACT, RTL	RTL
MVP – Assembly SysC	Platform Assembly / Register	IP-XACT, SystemC	SystemC / C
MCB, MCP, MLT - Documentation	Search, Publish, Trace	IP-XACT, Excel	Reports (HTML / PDF)

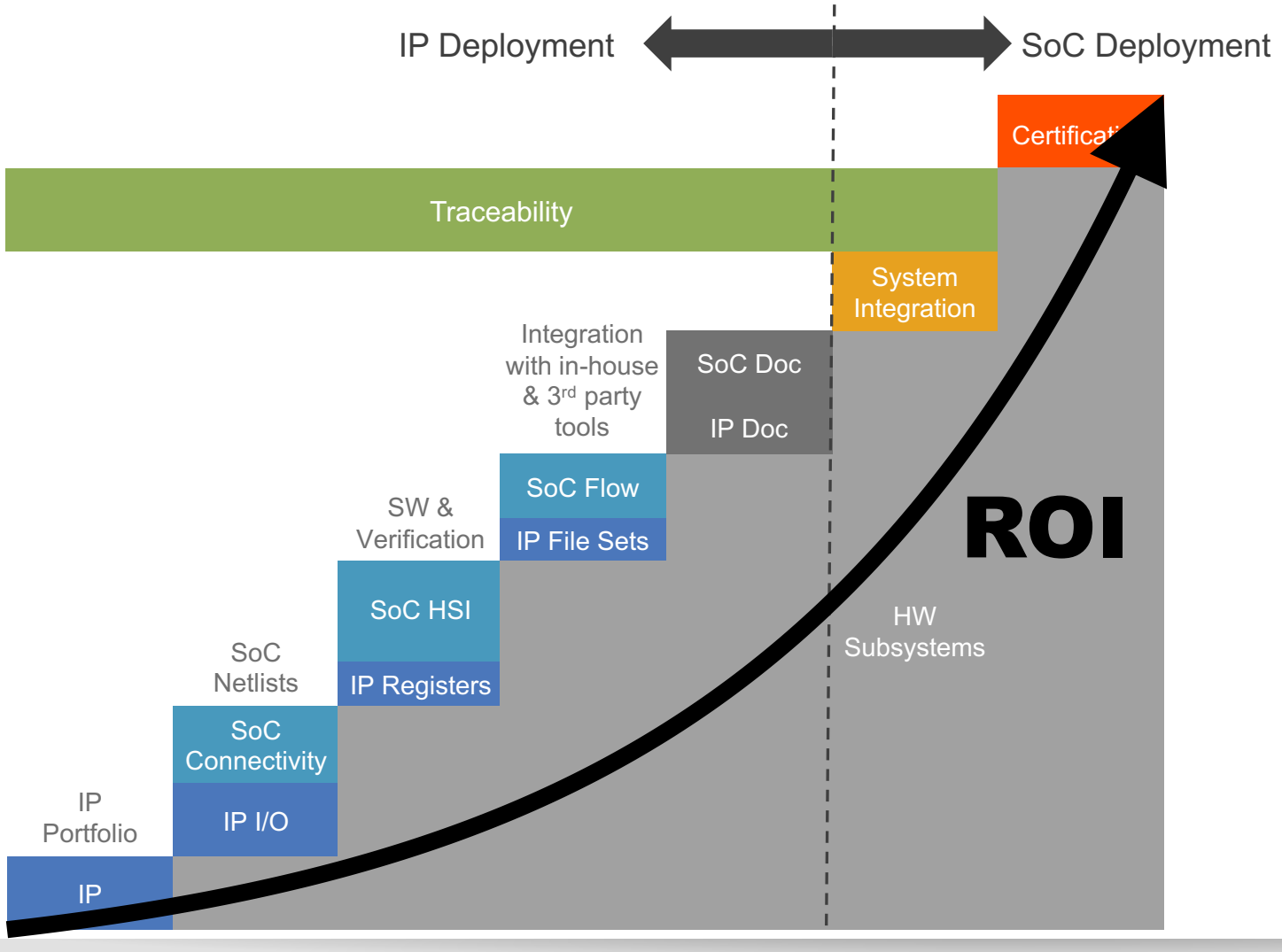
Incremental adoption of IP deployment



IP-XACT structure allows for an incremental adoption of the standard for the various needs.

- RTL & SystemC follow similar approach. SystemC cheaper than RTL
- Connectivity & HSI steps are interchangeable
- Flow step is not mandatory & can work with connectivity or HSI
- Documentation can start at any point.

Exponential ROI when adopting all capabilities

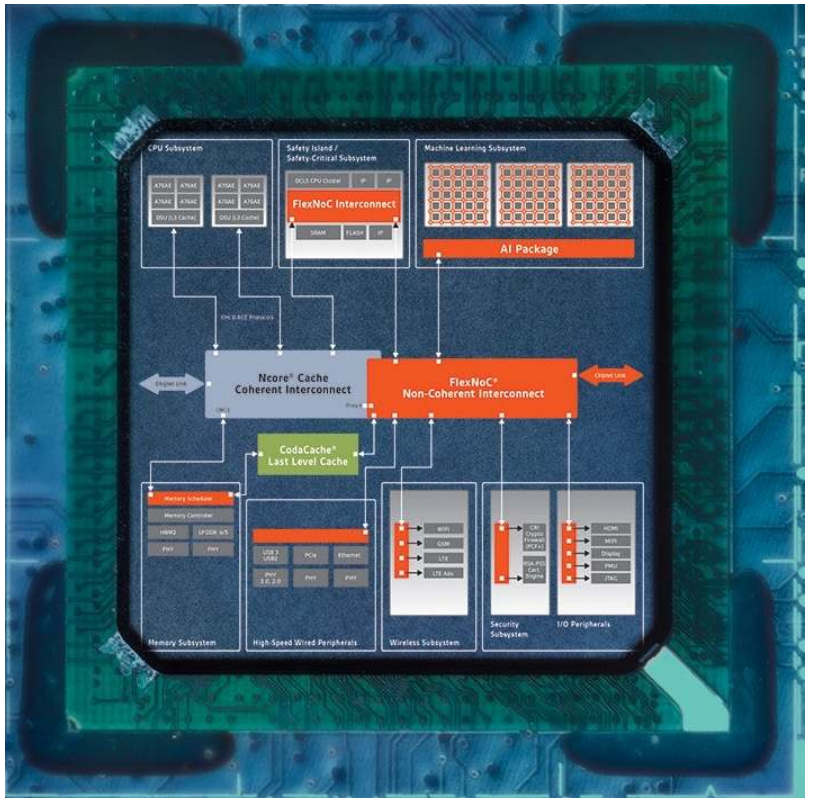


ROI grows as usage increases

- Building a standard base database, each step able to capitalize on the previous step
- Adding new capabilities becomes easier and less expensive because a lot can be reused from previous steps
- This enables our customers to enjoy an exponential ROI when adding new capabilities.

Arteris IP – The Best Way to Assemble IP Blocks into SoCs

- Performance & Productivity with market leading PPA
- Deep interconnect IP technology & product portfolio
- Continuous Interconnect Technology Delivery
- Integrated, IP-XACT based IP Deployment Platform
- Experienced Global Support
- Proven Products shipping in billions of systems



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Thank you!

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