Advanced Packaging Technologies for Heterogeneous Integration (HI)

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Executive Summary

Part 1 : The Package as a Compact HI Platform : Some Key Elements

• On-Package Interconnects
• High Bandwidth Signaling
• Power Delivery
• Thermal Management
• Assembly Processes
• Materials & Design Tools

Part 2 : Product implementations using Advanced Packaging Technologies
Outline

• Introduction – The Package as a Compact HI Platform
• On Package Interconnects & High Bandwidth Signaling
• Power Delivery Architectures
• Thermal Management
• Assembly Process, Materials and Design Tools
• Summary
Increased Interest in HI is Driven by

Need to Mix and Match of Diverse IP Optimized on Different processes

Escape from Reticle Limits

Need for Proximate Memory with a High BW Low Power Interface

Additionally, Yield Resiliency and Time to Market Advantages Make On-Package HI Attractive
The Package is a Compact HI Platform For Several Interesting Use Cases

Sources: Intel Architecture Day (2021) & ERI Summit (2020). The CHIPS work is supported by the DARPA MTO office (DARPA CHIPS Program)
The Package as a HI Platform – Key Focus Areas

- Power-efficient, High Bandwidth On-Package IO links
- Enable a diversity of off-package IO protocols
- Deliver noise isolation for single ended and differential signals
- Manage increasing cooling demands
- Support complex power delivery architectures
- Meet diverse application functionality ranging from high performance servers to flexible, wearable electronics
- Meet a broad spectrum of reliability requirements for different market segments and applications
- Provide cost effective, high precision quick turn assembly
On-Package Interconnects & High Bandwidth Signaling

- Power-efficient, High Bandwidth On-Package IO links
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High Density Interconnects: Physical Metrics

- Wiring Density increases Require Wire (aka IO)
  Width, Space & Pad reduction (Zero Pad Ideal)
- Bump Density Increases Require Bump Pitch Shrinks

R. Mahajan et al., "Embedded Multi-die Interconnect Bridge (EMIB) -- A High Density, High Bandwidth Packaging Interconnect," 2016 ECTC
Current State of Advanced Packaging (Intel Centric View)

- **EMIB**
- **Foveros**
- **EMIB-Foveros**
Planar Interconnects: MCP Landscape

Focus: Increased Interconnect Density + Improved Power Efficiency for Increased BW
Vertical Interconnects : MCP Landscape

Transition from Solder Based Interconnects to Cu-Cu interconnects needed with shrinking Bump Pitch*

*Li et al. “Scaling Solder Micro-Bump Interconnect Down to 10 μm Pitch for Advanced 3D IC Packages” ECTC 2021
Blending 2D and 3D

• Architecture for >> reticle sized die + High-Density Bridge links
• Increased Partitioning Opportunities in X, Y and Z
I/O Bandwidth & Speed Scaling Trends

- Growing Network & Memory (BW + Speed) Demand
- As peak FLOPS grow BW will need to keep up
- BW Demand poses significant challenge for the physical and signaling characteristics of the package interconnect

Reproduced with permission from Ethernet Alliance
Enable high bandwidth density connection between dies on an ‘advanced package’ with simple I/O circuits and low power consumption with limited reach.

R. Mahajan et al., "Embedded Multi-die Interconnect Bridge (EMIB) -- A High Density, High Bandwidth Packaging Interconnect," 2016 ECTC
Interconnect Scaling to Enable Bandwidth Scaling

- Peripheral Interconnects for Solder Based 2D Architectures

<table>
<thead>
<tr>
<th>Generations</th>
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<td>250</td>
<td>500</td>
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<td>Package Technology</td>
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<td></td>
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<td>667</td>
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<td>IO/mm²</td>
<td>331</td>
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<td>Signaling Speed</td>
<td>Gbps</td>
<td>2</td>
<td>3</td>
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- Peripheral Interconnects for 2D Architectures with Aggressive pitch Scaling

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<td>IO/mm²</td>
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<td>Signaling Speed</td>
<td>Gbps</td>
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Interconnect Scaling to Enable Bandwidth Scaling

• Area Interconnects for 3D Architectures

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<tr>
<td>Package Technology</td>
<td>Minimum Bump Pitch (µm)</td>
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<td>30</td>
<td>20</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>IO/mm²</td>
<td>625</td>
<td>1111</td>
<td>2500</td>
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<tr>
<td>Signaling Speed</td>
<td>Gbps</td>
<td>1.6</td>
<td>1.8</td>
<td>1.6</td>
<td>1.8</td>
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Power Delivery

- Power-efficient, High Bandwidth On-Package IO links
- Enable a diversity of off-package IO protocols
- Deliver noise isolation for single ended and differential signals
- Manage increasing cooling demands
- Meet a broad spectrum of reliability requirements for different market segments and applications
- Support complex power delivery architectures
- Meet diverse application functionality ranging from high performance servers to flexible, wearable electronics
- Provide cost effective, high precision quick turn assembly

Meet diverse application functionality ranging from high performance servers to flexible, wearable electronics.
The Evolution of Power Management

• **Historical Approach (1980s to early 2000s)**
  - Frequency scaling → Faster (& leaky) transistors enable higher frequency
  - Scale $V_{th}$ & device dimensions
  - Increased leakage and active power

• **Shift to Multi-Core (mid 2000s)**
  - Slow down $V_{th}$ scaling & Process improvements to control leakage
  - Slow down frequency scaling
  - Add more cores for performance

Number of power rails has steadily gone up to improve power management
FIVR – Fully Integrated Voltage Regulator

FIVR was introduced by Intel® on the 4th generation Core™ Microprocessors

- Steps down the 1.8 V Vin to a range of output voltages (0.5 – 1.3V)
- The number of FIVR phases on a microprocessor can range from 50 to 300

A single MBVR converts the incoming platform power supply voltage to 1.8V
Efficiency on First Generation FIVR

First generation of FIVR achieved an efficiency of 90% at full $V_{out}$ (1.08 V)
- First generation FIVR ACI had a high Q-factor due to a large XY footprint and a 700um core

- Process scaling reduces core area → Shrinks the ACI XY footprint
- The push to thin and light devices has reduced the substrate core thickness hurting ACI performance
Magnetic Inductor Arrays

The 10th generation Intel® Core™ microprocessors used a number of MIA modules for the different voltage domains

- The use of magnetic inductors helps recover the loss of efficiency due to ACI area scaling
The Package as a HI Platform – Key Focus Areas

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Key challenges:
• Die-die thermal resistance, thermal cross-talk between neighboring die, and higher power density due to stacked active die → The combined effect results in lower cooling capability for 3D packages compared to 2D packages.

How Intel manages Thermals:
• Low resistance die-to-die thermal interfaces (Foveros Omni and Foveros Direct packages).
• Best in class metallic thermal interface material (TIM1) between die and integrated heat spreader (IHS).
• Thermally optimized Si floorplan and package architectures. Co-design of Si and Package for improved thermals.
Assembly Process, Materials and Design Considerations

- Power-efficient, High Bandwidth On-Package IO links
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- Support complex power delivery architectures
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- Meet a broad spectrum of reliability requirements for different market segments and applications

INC.
Assembly and Test Technology Development Scope

Assembly TD Focus: High functionality, High Yield, High Quality & Reliability
Heterogeneous packaging: Challenges and opportunities

**Better materials**
- UF/mold: Flow, Reliability, Warpage
- Fluxes: joint quality/cleanability
- Thermal interface materials

**Improved Electrical**
- Bump Current carrying capability
- HSIO and Power Delivery
- Design co-optimization

**Fine pitch interconnect joint yield**
- Die-Die, Die-Wafer, Die-Substrate
- Improved alignment/bump Coplanarity
- Stacked die coplanarity

**Advanced substrates**
- Improved bump coplanarity
- Fine pitch/Multi diameter bumping
- High density routing

**Acceptable Reliability**
- Temperature cycling
- Electromigration
- Temperature/humidity/Bias

**External IP/die/pkg integration**
- Passivation/bump compatibility
- Design rule/Design co-optimization

Equipment/ Material/Process/ Design Co-optimization key to Heterogeneous Assembly & Packaging
Advanced Substrates: Challenges & Opportunities

High Density Routing:
Advanced Patterning, Via Formation, Etch
Materials: Better photoresists
Via fill/plating chemistries

Large Package Form Factors:
Panel/Wafer Processing

Chip to Chip Bridge:
EMIB: High Precision Embedding

Fine Pitch Assembly:
Planarization Technologies to enable Planar bumping & Buildup layers

Fine Pitch Heterogeneous Bumping:
Advanced Buildup/RDL Cu & Bump Plating-tools/chemistries

High BW- HSIO:
Materials: Advanced Dielectric Materials Smooth Cu/Barrier Layers

Equipment/ Material Advances in Substrate Panel Processes key to Heterogeneous Integration
Today there is Broad and Growing consensus that Heterogeneous Integration (HI) is a key enabler of performance moving forward.

- On-Package Integration, using Advanced Packaging Architectures for Compact, Power Efficient, High Bandwidth Platforms is a key HI Element
- Number of Innovative package architectures are available today to facilitate power efficient, high bandwidth die-die interconnects on package → There is a roadmap to scale these interconnects in all three dimensions
- Delivering a clean power supply is important to optimize microprocessor performance
  - The increase in power rails & overall power levels introduces new power delivery challenges
  - Development of high efficiency, high density, high voltage IVRs will be critical to meet the requirements of future high-performance microprocessors
- Thermal Management requires Continued Materials and Co-Design Focus
- Continued Scaling of Advanced Packaging requires focus on multiple aspects including interconnect design, high-speed signaling, power delivery, thermal management, materials, assembly and process design

Summary
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Advanced Packaging Technologies: Product Implementations

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Acknowledgments: Ram Viswanath, Mark Gardner, Jan Krajniak, Luke Garner, Pat Stover, Chris Baldwin, Babak Sabi
Current State of Advanced Packaging (Intel Centric View)
EMIB Embedded Multi-Die Interconnect Bridge

- Localized high-density wiring
- Multiple Bridges, Multiple Bridge Sizes and Bridge Technologies
- Bridge Mix and Match $\rightarrow$ Enhanced Design Flexibility
- Bridge silicon costs < Silicon interposer
  - No TSVs, Significantly less silicon area
- Die from Different Foundries
- Large Overall Die Area enabled
### Sapphire Rapids - EMIB Implementation

<table>
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<tr>
<th>Attribute</th>
<th>SPR XCC</th>
<th>SPR HBM</th>
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<tr>
<td>Top Die Count</td>
<td>4</td>
<td>4, + 4 HBM2E</td>
</tr>
<tr>
<td>Max Top Die Size</td>
<td>~400 mm²</td>
<td>~400 mm²</td>
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<tr>
<td>EMIB Pitch</td>
<td>55µm</td>
<td>55µm</td>
</tr>
<tr>
<td>Core Pitch (minimum)</td>
<td>100µm</td>
<td>100µm</td>
</tr>
<tr>
<td>Memory (HBM)</td>
<td>N/A</td>
<td>4x 8H HBM2E</td>
</tr>
<tr>
<td>Package size</td>
<td>78 x 57 mm</td>
<td>100 x 57 mm</td>
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<tr>
<td>EMIB count</td>
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<td>14</td>
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# EMIB Link Capability

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<th>Intel MDF</th>
<th>Intel OPIO</th>
<th>Improvement due to EMIB</th>
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<tbody>
<tr>
<td>Packaging Tech</td>
<td>EMIB</td>
<td>Standard 2 routing layers</td>
<td></td>
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<tr>
<td>Bump Pitch (µm)</td>
<td>55</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>Pin Speed (Gbps)</td>
<td>5.4</td>
<td>8 – 16</td>
<td></td>
</tr>
<tr>
<td>Shoreline BW density (GBps/mm)</td>
<td>196</td>
<td>34.5 – 69</td>
<td>5.68x – 2.84x</td>
</tr>
<tr>
<td>Areal BW density (GBps/mm²)</td>
<td>158</td>
<td>36.7 – 73.4</td>
<td>4.3x – 2.15x</td>
</tr>
<tr>
<td>PHY power efficiency</td>
<td>0.5</td>
<td>1.5-2.0</td>
<td>3x – 4x</td>
</tr>
</tbody>
</table>

- Intel MDF was announced in Semicon West 2019.
- Intel OPIO 8Gbps was used in a Client in 2013. Higher speeds were developed in an internal study.
Intel Foveros: High Density 3D

Compact Active Die Stacking: Initial Offering is Single Tile on Base die @ 50μm pitch.

We are systematically Scaling tile count, Bump pitch.

2. W. Gomes et al., “8.1 Lakefield and Mobility Compute: A 3D Stacked 10nm and 22FFL Hybrid Processor System in 12×12mm2, 1mm Package-on-Package,” 2020 ISSCC
Ponte Vecchio

SOC

>100 Billion Transistors
47 Active Tiles
5 Process Nodes
## Ponte Vecchio

### Attribute PVC 2T

<table>
<thead>
<tr>
<th>Attribute</th>
<th>PVC 2T</th>
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<tr>
<td>D2D Pitch</td>
<td>36µm</td>
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<tr>
<td>Active Top Die Count Per Stack</td>
<td>16</td>
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<tr>
<td>Max Active Top Die Size</td>
<td>41mm²</td>
</tr>
<tr>
<td>Base Die Size</td>
<td>650mm²</td>
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<tr>
<td>EMIB Pitch</td>
<td>55µm</td>
</tr>
<tr>
<td>Core Pitch (min)</td>
<td>100µm</td>
</tr>
<tr>
<td>Memory (HBM)</td>
<td>8x</td>
</tr>
<tr>
<td>Package size</td>
<td>(77.5 x 62.5) mm</td>
</tr>
<tr>
<td>EMIB count</td>
<td>11</td>
</tr>
</tbody>
</table>
Continued leadership in advanced packaging

**Embedded Multi-die Interconnect (EMIB)**
- bump pitch ≤ **55 microns**
- leads industry
- first 2.5D embedded bridge solution
- products shipping since 2017

**Foveros Technology**
- bump pitch **50-36 microns**
- wafer-level packaging capabilities
- first-of-its-kind 3D stacking solution

**Foveros Omni**
- bump pitch ~**25 microns**
- next gen Foveros technology
- unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

**Foveros Direct**
- bump pitch < **10 microns**
- direct copper-to-copper bonding for low resistance interconnects
- blurs the boundary between where the wafer ends and the package begins
Packaging Innovations In The Near Future: Foveros Omni and Foveros Direct

- Rich Interconnect Portfolio allows greater mix-and-match and better/independent interconnect optimization for Power and IO

- Pitch Scaling from $25\mu m \rightarrow \leq 10\mu m$ leads to an order of magnitude increase in IO/mm² ($1600 \rightarrow \geq 10,000$)
Key Messages

- Several Innovative Packaging Architectures are available today for Scaling in all 3 directions – In Today’s talks we have focused mainly on the physical implementations.

- Intel is using them in Client, Server and Discrete Graphics products to provide unprecedented levels of Heterogeneous Integration.

- The next generation of Innovations in HI will offer increased partitioning opportunities with an enhanced interconnect portfolio and significant increases in interconnect density.
Thank you!

“Something is going to happen.”
“What is going to happen?”
“Something __________.”

bit.ly/2VEW6Dt
References

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