ADVANCED PACKAGING

ENABLING MOORE’S LAW’S NEXT FRONTIER THROUGH HETEROGENEOUS INTEGRATION

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Many Well-known Technology Challenges | Slowing of Moore’s Law, Cost Increases, Die-size Limits, Power
FUTURE OF COMPUTING

Compute Demand

- Compute demand increasing
- Significant barriers to traditional scaling

Domain Specific Accelerators

- Higher efficiency domain specific accelerators required

Modular Design

- Modular design supported by advanced packaging required

Die Size Increases over Time

Market dynamics limited
CHIPLETS BACKGROUND

Historically, except for the largest systems, Moore’s Law was sufficient to meet compute needs

Current trends require a new approach

However, chiplets not free
- Additional area for interfaces, replicated logic
- Additional design effort, complexity
- Past methodologies less suited for chiplets

2X Device Functionality
Costs > 2X Silicon Area
HIGH-LEVEL APPROACH TO CHIPLETS

Many More Functional SoCs
Ability to mix and match at a finer grained level
MODULAR DESIGN PROGRESSION

Key Parameters for Modular Chiplet Integration

- Cost and volume capability – addressing the world’s compute needs requires scalable, cost-effective solutions
- Bandwidth density – area overhead of die-die communication must be minimized
- Energy per bit – tighter integration means more bits/s. Power cost must be minimized
PACKAGE ARCHITECTURE GOALS

ENABLING A FLEXIBLE PACKAGING APPROACH

- Enable performance, power, area, cost (PPAC) for high-performance leadership products
- Heterogeneous architectures for configurable, segment-specific optimization
- Maximize product yield by enabling smaller, low-interconnect-overhead chiplets
No single package architecture works for all products - choice based on product PPAC
FINDING THE OPTIMAL SOLUTION

Chiplet package architecture selection requires balancing a complex equation...

Architectural need for bandwidth, die partition options and package technology create a multi-disciplinary optimization equation
AMD LEADERSHIP PACKAGING

2015
2.5D HBM
Led Industry in HBM, 2.5D & Chiplet Architecture

2017
MULTICHP MODULE

2019
CHIPLETS

2021
3D CHIPLETS
(Chiplet + Advanced 3D Stacking)
Aggressive Roadmap for Chiplet & 3D Integration
AMD PACKAGING ROADMAP

- **Linear Interconnect Density (Wires/mm/layer)**
- **Area Interconnect Density (Wires/mm²)**

**Graphical Elements:**
- 2D MCM (GMI)
- 2.5D Si Interposer
- 3D Chiplets

**Note:**
- Highest Performance, Lowest Power and Area
AMD 3D CHIPLET TECHNOLOGY
AMD 3D CHIPLET TECHNOLOGY

C4 and Micro Bump 3D illustrations are hypothetical.
ENGINEERING THE 3D CHIPLET ARCHITECTURE

- Structural silicon
- 64MB L3 cache die
- Direct copper-to-copper bond
- Through Silicon Vias (TSVs) for silicon-to-silicon communication
- Up to 8-core "Zen 3" CCD
HYBRID BONDING

HYDROPHILIC DIELECTRIC-DIELECTRIC BONDING + DIRECT CU-CU BONDING

TECHNOLOGY/DESIGN CO-OPTIMIZED IN DEEP PARTNERSHIP WITH TSMC
**OTHER 3D ARCHITECTURE**

- Micro Bump (50u → 36u pitch)
- ~50u tall TSV

**AMD 3D CHIPLETS**

- Hybrid Bond (9u pitch)
- Back End Like TSV

>3X
Interconnect Energy Efficiency
Compared to Micro Bump 3D

>15X
Interconnect Density
Compared to Micro Bump 3D

**BETTER SIGNAL/POWER**

Lower TSV capacitance, inductance
Compared to Micro Bump 3D

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Based on AMD engineering internal analysis, May 2021. See endnotes.
POWER AND AREA BENEFITS

>3X POWER BENEFIT
Compared to Micro Bump 3D

Interconnect power (W)

- **Micro Bump 3D architecture**
- **AMD 3D Architecture**

130µ
9µ
50µ
3D CHIPLET TECHNOLOGY
15% FASTER GAMING ON AVERAGE

UP TO 1.18X
DOTA 2 (Vulkan®)

UP TO 1.12X
Gears V (DirectX® 12)

UP TO 1.25X
Monster Hunter World (DirectX® 11)

UP TO 1.04X
League of Legends (DirectX® 11)

UP TO 1.17X
Fortnite (DirectX® 12)

Ryzen™ 9 5900X / 4.0 GHz Fixed Frequency
12-Core 3D Chiplet Prototype / 4.0 GHz Fixed Frequency

ADVANCED PACKAGING ENABLING GENERATIONAL PERFORMANCE GAINS

Based on AMD engineering internal analysis, May 2021
FUTURE OF 3D STACKING

ADVANCED PACKAGING CAN ENABLE INTEGRATION SCHEMES
NOT POSSIBLE WITH MONOLITHIC DESIGNS

Based on AMD engineering internal analysis, May 2021
ACCELERATING WITH ADVANCED PACKAGING
DRIVING HIGH-PERFORMANCE COMPUTING FORWARD

Linear Interconnect Density (Wires/mm/layer)

Area Interconnect Density (Wires/mm$^2$)

Highest Performance, Lowest Power and Area

2D MCM (GMI)

2.5D Si Interposer

3D Chiplets
ACCELERATING WITH ADVANCED PACKAGING

DRIVING HIGH-PERFORMANCE COMPUTING FORWARD

SILICON PROCESS SLOWING  ADVANCED PACKAGING INNOVATIONS CRITICAL

ADVANCED PACKAGING LEADERSHIP
ENDNOTES

AMD 3D Chiplet Technology

Competition 3D architecture picture from SystemPlus. Intel Core i5-L16G7: the first utilization of Intel’s Foveros Technology with Package-on-Package configuration in a consumer product.. https://www.systemplus.fr/reverse-costing-reports/intel-foveros-3d-packaging-technology/

3D Chiplet Gaming Demo And Performance Chart

Testing by AMD performance labs as of April 28, 2021 based on the average FPS of 32 PC games at 1920x1080 with the High image quality preset using an AMD Ryzen™ 9 5900X processor vs. 12-Core 3D Chiplet Prototype. Results may vary. R5K-078.
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