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A CORDIC-based Trigonometric Hardware Accelerator with Custom Instruction in 32-bit RISC-V System-on-Chip

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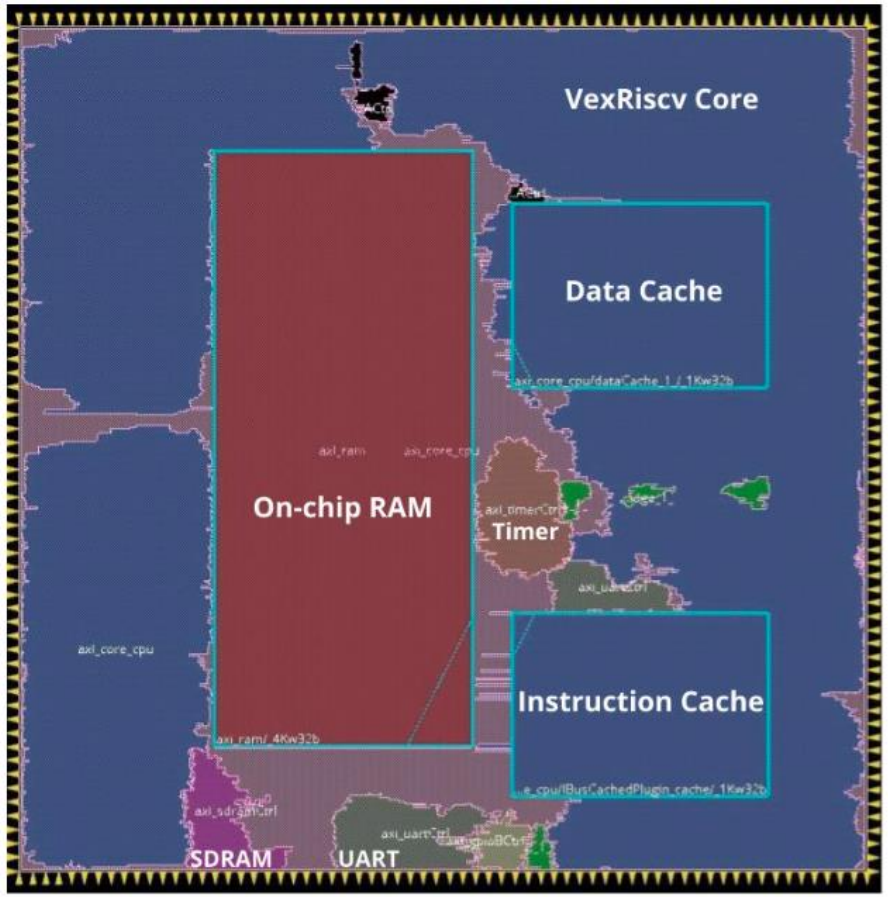
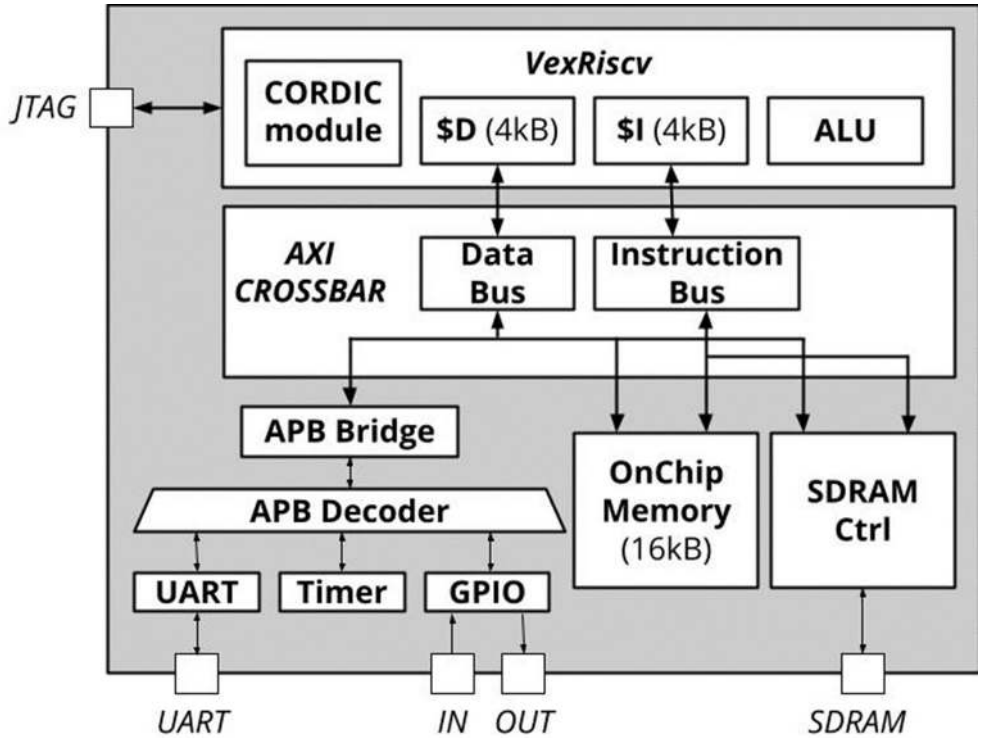
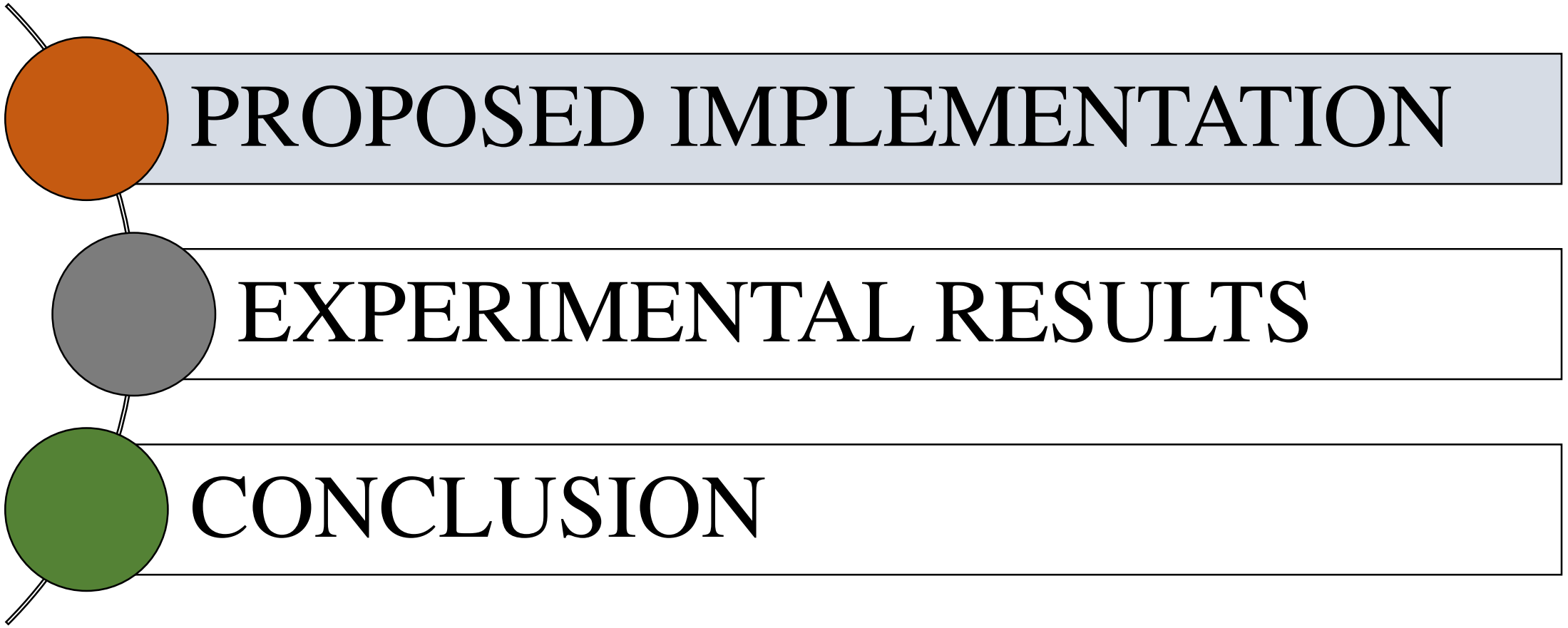
Introduction (1/1)

This poster presents a 32-bit Reduced Instruction Set Computer five (RISC-V) microprocessor with a COordinate Rotation DIgital Computer (CORDIC) algorithm accelerator. The implemented core processor is the VexRiscv CPU, an RV32IM variant of the RISC-V ISA processor. Within the VexRiscv core, the CORDIC accelerator was connected directly to the Execute stage. The core was placed in Briey System-on-Chip (SoC) and was synthesized on Field Programmable Gate Array (FPGA) and on Application Specific Integrated Chip (ASIC) level with the cell logic of ROHM-180nm technology





OUTLINE


PROPOSED IMPLEMENTATION
EXPERIMENTAL RESULTS
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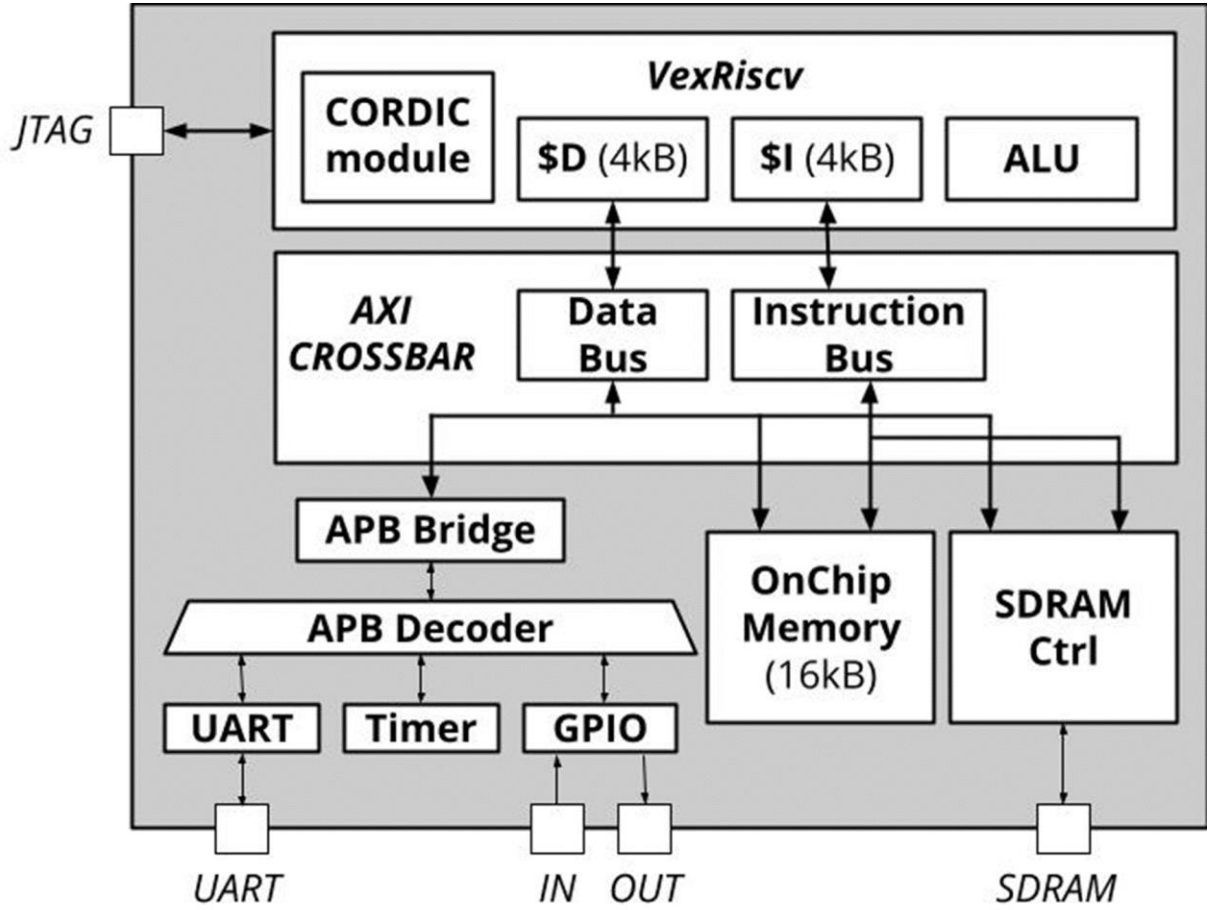
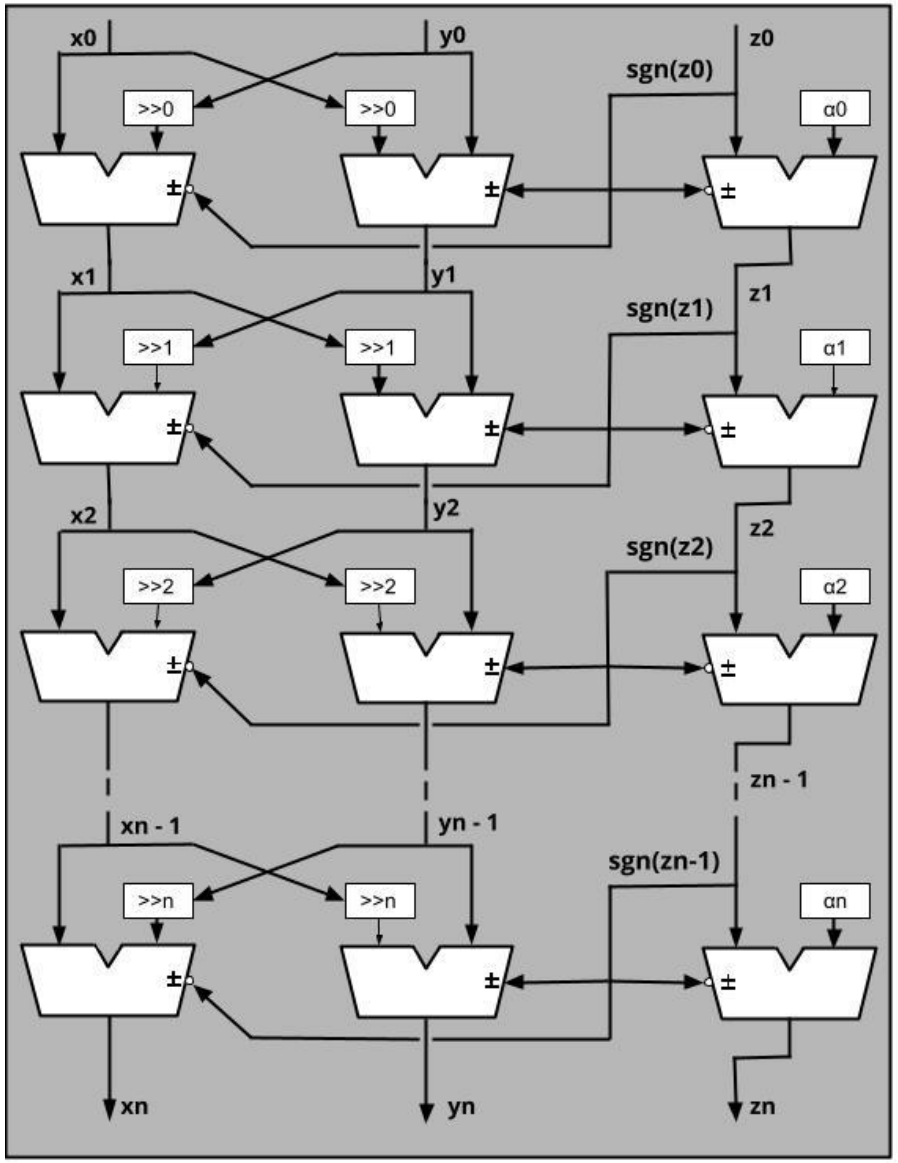
PROPOSED IMPLEMENTATION(1/3)



Briey SoC Architecture

- 32-bit RV32IM RISCV- CPU, 4KB I-Cache, 4KB D-Cache and Arithmetic Logic Unit.
- AXI connect to SDRAM, ABP3 Bridge and 16kB on-chip RAM.

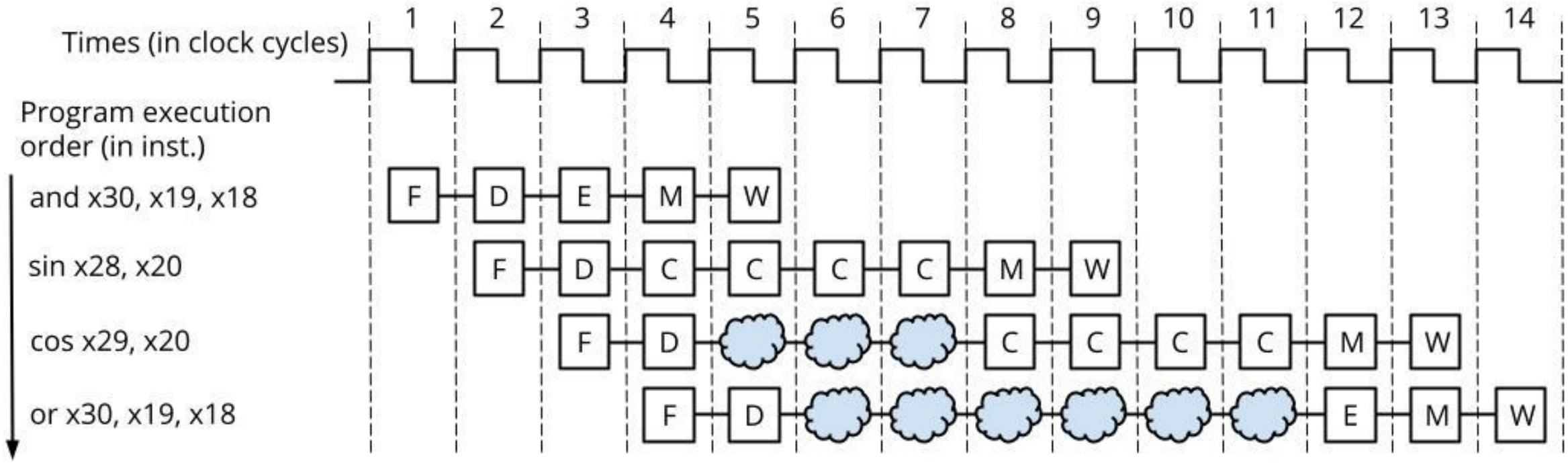
PROPOSED IMPLEMENTATION(2/3)



CORDIC Bit-parallel, unrolled Structure

- Central unit of computation in the accelerator.
- Bit-parallel, unrolled structure, which only uses adders, subtractors, and shifters
- $x_0 = 1024/K$, $y_0 = 0$ and $z_0 = angle$
- Input angle will be processed before being fed into the CORDIC circuit

PROPOSED IMPLEMENTATION(3/3)

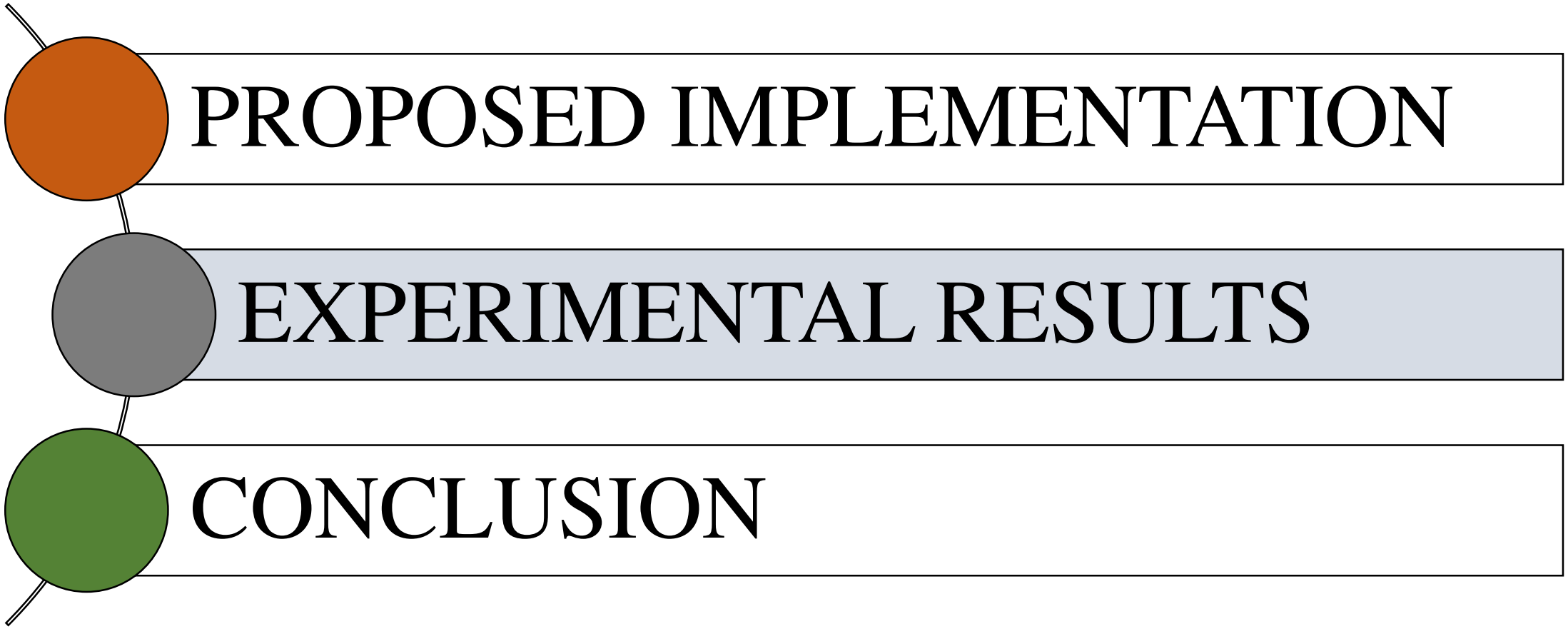


Multiple-clock-cycle pipeline diagram of the custom instructions.
F: Fetch, D: Decode, E: Execute, M: Memory, W: Write Back, C: CORDIC execution.

- Each CORDIC instruction requires eight clock cycles to complete (4 cycles on Execute)

=> Increase latency by three clock cycles

OUTLINE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EXPERIMENTAL RESULTS (1/3)

Table I. Hardware utilization summary in FPGA implementation.

	LUTs	FFs	BRAM
Briey SoC	5,377	3,271	206,592
VexRiscv Core	3,999	1,639	75,264
Data Cache	168	150	35,584
Instruction Cache	37	97	33,584
CORDIC module	800	186	0
JTAG	106	138	0
On-chip RAM	55	27	131,072
SDRAM Controller	384	308	0
GPIO	15	144	0
UART	184	110	256
Timer	251	222	0

FPGA resource utilization

- Obtained on the Altera DE2-115 FPGA Development Kit with the chip of EP4CE115F29C.
- CORDIC accelerator increased system overhead by 25.13% and 8.41% for LUTs and FFs.

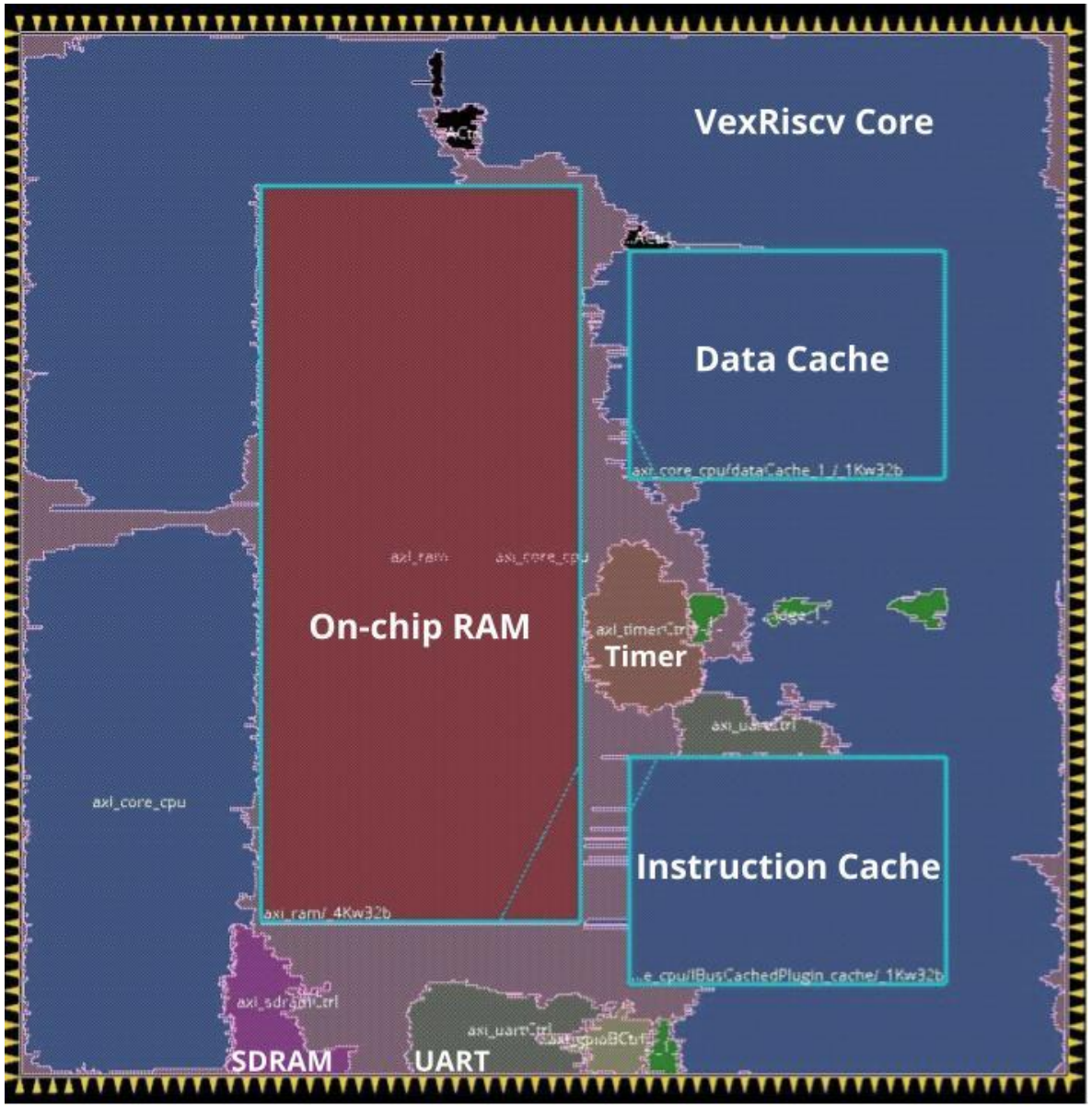
EXPERIMENTAL RESULTS (2/3)

Table II. Comparison between software and hardware implementation.

	VexRiscv with CORDIC	VexRiscv without CORDIC
Implementaion	FPGA	
Approach	Accelerator	Software
Speed (clock cycles)	8	3,314
Maximum Frequency(MHz)	54.07	72.63
Processor	VexRiscv	
CORDIC Structure	Bit-parallel unrolled	NA

- Software:
  - Test program written in C
- Hardware:
  - Use inline assembly to call the CORDIC custom instruction
- Compiled using the GNU Compiler Collection (GCC) RISC-V toolchain.
- CORDIC accelerator reduces the maximum frequency by about 25%

EXPERIMENTAL RESULTS (3/3)



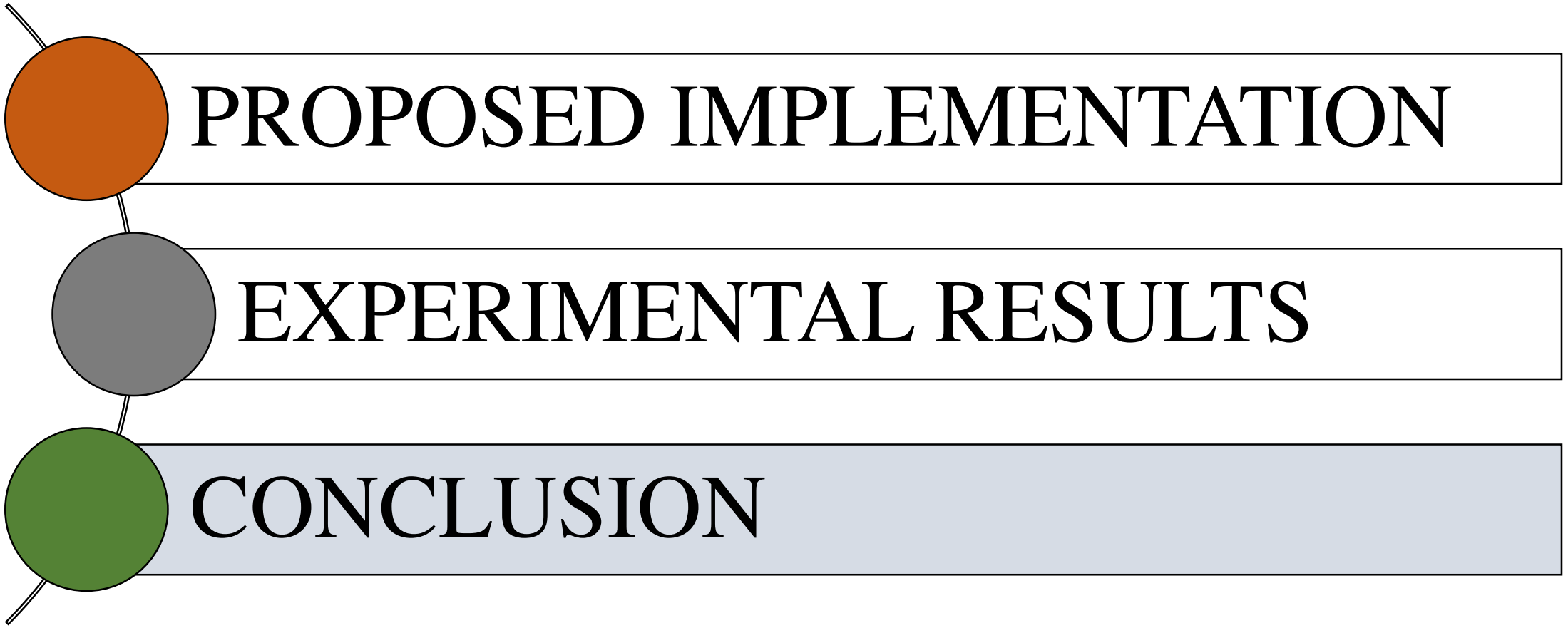
VLSI implementation configuration

- Process: ROHM-180nm
- Core area: 308,101 NAND2-gate, 3-mm^2
- Power *(at 100MHz)*: 649-mW
- F_{Max}: 107-MHz

Table III. Utilization summary in CMOS 180-nm implementation.

	Area		Gate
	μm^2	%	(NAND2)
Briey SoC	2,981,434	100.00	308,101
VexRiscv Core	1,769,722	59.35	182,883
Data Cache	585,506	19.64	60,506
Instruction Cache	579,081	19.42	59,842
CORDIC module	92,120	3.09	9,520
JTAG	11,754	0.39	1,215
On-chip RAM	987,507	33.12	102,049
SDRAM Controller	28,376	0.95	2,932
GPIO	27,624	0.93	2,853
UART	40,646	1.41	4,200
Timer	30,992	1.07	3,203

OUTLINE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CONCLUSION (1/1)

- RV32IM VexRiscv CPU with a trigonometric functions accelerator using CORDIC algorithms was presented.
- The complete System-on-Chip was built and tested on DE2-115FPGA Development Kit.
- The VLSI implementation is synthesized in the ROHM-180nm process with 3-mm^2 area result.
- The maximum frequency the system can reach on FPGA is 54.67-MHz and on ASIC is 107-MHz.
- The power consumption is 649-mW at 100-MHz

THANK YOU

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Acknowledgement
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