

SOT-MRAM – Third generation MRAM memory opens new opportunities

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'Generational' Advances in MRAM \rightarrow SOT-MRAM

	<u>Gen 1</u> 'Toggle'		<u>Gen 2</u> Spin Transfer Torque – 'STT'		<u>Gen 3</u> Spin Orbit Transfer– 'SOT'	
	 Full NVM retention >10¹⁵ r/w cycles 35ns cycle time 		 Full NVM retention (with reflow) DRAM speed behind DDR ~10⁹-10¹⁰ R/W cycles 50ns Write/25ns Read 		 Full NVM retention (with reflow) SRAM speed behind standard parallel interface >10¹⁵ R/W cycles 5-10 ns cycle time, improving 	
	 130nm CMOS 35ns 16 Mbit max density 		 28 nm CMOS 50/25ns 1Gbit max density 		 22 nm CMOS to start 5-10ns and faster 1+ Gbit max density 	
	 No tunnel oxide write current Standalone 		 High tunnel oxide write current Embedded NVM Standalone 'RAM' 		 No tunnel oxide write current Embedded NVM Embedded RAM Standalone 	
JUMP THE ENDURANCE CONSTRAINT						

SOT vs STT MRAM – Key Differences



SOT value add wrt STT

- + Unlimited write endurance
- + Intrinsically fast write (5-10x faster)
- + Write energy 5-10x reduced
- + Lower write voltage
- + Endurance doesn't 'compete' with retention speed
 → simultaneously meets RAM & NVM requirements
- Slight memory area adder

SOT & STT common figures

o Immune to ionizing radiation

- No data retention leakage current
- Back-end of line MTJ device process flow
- o Same foundry MRAM equipment & process flow

SOT MRAM as CPU Cache 22nm CMOS and smaller → 64-512 Mbyte density



Considerations for use as CPU Cache

- R/W cycle time versus Retention Period
 - Option 1 : Fully 'static' data (like NVM) Slowest R/W cycle, no data scrub
 - Option 2 : With 'data scrub' (like DRAM refresh) Higher scrub frequency → faster R/W cycle
 Note : 'Cache flush' can provide same cycle time benefit as 'data scrub'

- R/W cycle = 5-10ns, with path to <5ns</p>
- Retention / Scrub 'sweet spot' Likely 1 day 1 month
- Other features
 - Unlimited write endurance
 - Sub 0.1-1 pJ/bit write energy
 - > No leakage power, immune to ionizing radiation
 - Area/bit < SRAM</p>
- 2 possible integration paths:
 - 'Conventional' full die integration
 - Stacked die, with TSV



Separate program & data memory



Traditional MCU Architecture



Benefits of SOT MRAM for XiP in Microcontrollers

Results of 'pro forma' system estimate to typical architecture in IOT, Portable Printer, Camera

- Power
 - Overall power reduced by 2x to >10x
 - Write energy/bit scaled down reduction in write time >10³
 - Removal of block-data transport
- Cost
 - Total chip area reduced by 20-50%
 - SOT bit < SRAM bit
 - Fewer incremental mask steps compared to e-Flash
 - Single memory block on chip = no duplicate storage for run-time execution
- Performance
 - Total execution speed improved by 25% to >90%
 - Write speed improvement by 10³
 - No remapping/swapping of data block

Why improvements ?

- Two memory blocks collapse to one
- Data block swapping to fit code in RAM disappears
- Power down data storage cycle disappears
- Flash 'overhead' gone
 - Low energy word-wise re-write at clock speed, rather than slow block erase
 - NVM writes at system clock speed, rather than microseconds required for slow Flash write



- Value in 'edge' and 'cloud' architectures still emerging
- Direct impact in edge devices for 'feature map' operation, where the memory operates similar to a cache/working-memory
 - Same benefits as in CPU cache applications, with added benefit of reduced active power compared to external DRAM
- Edge devices are sensitive to endurance, write power/energy, write speed
 - Flash is unacceptable
 - SOT ~5-10x better than STT MRAM in energy per write and write speed
 - SOT write endurance is unlimited, where STT write endurance ~10⁹-10¹²
- New value in NV-SRAM \rightarrow architectural opportunities
 - ~10ns R/W cycle or better

Summary



SOT is a straightforward extension of today's 'in production' MRAM technologies running in major foundries

First memory technology to genuinely have the capability to **converge both SRAM and NVM** characteristics in advanced CMOS nodes (≤28nm)

Power, cost, and performance benefits of SOT are compelling

SOT is still in development, but look for market visibility to begin around 2024





The Memory Grail

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