Arm Neoverse N2: Arm’s 2\textsuperscript{nd} generation high performance infrastructure CPUs and system IPs

Andrea Pellegrini, Distinguished Engineer
Arm Infrastructure Line of Business

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Outline

• Roadmap
• Technical objectives and market targets
• Core architecture & uarchitecture
• System architecture & uarchitecture
• Performance projections
• Conclusions
Arm Neoverse Platforms Roadmap

**Platform features**

**IP Date**

- **Production**
  - 7nm
    - PCIe Gen4, DDR4, HBM2
    - CCIX 1.0
  - 7/5nm
    - PCIe Gen5, DDR5, HBM2e
    - CCIX 1.1
  - 5nm
    - PCIe Gen5, DDR5, HBM3
    - CCIX 2.0, CXL 2.0
  - 5/3nm
    - PCIe Gen5/6, DDR5, HBM3
    - CCIX next, CXL next

- **Now**
  - V1 Platform (Zeus)
    - N1+50% ST perf. uplift
    - SVE 2x256b, bFloat16
  - N2 Platform (Perseus)
    - N1+40% ST perf. uplift
    - SVE2 2x128b, bFloat16

**V-series**

- **Max**
- **ST Perf**
- **ML**

**N-series**

- **Perf/W**
- **Scale out**
- **5G**

**E-series**

- **Data efficiency**

**Poseidon Generation Platforms**

- +30% infra WL perf.
- ML/Vector uplift
- Greater core density

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Arm Neoverse Cloud-to-Edge Workload Positioning

**HPC Clusters and HPC in the Cloud**
- Cloud Data Centers
- High core count, high power HPC, enterprise & cloud CPUs
  - 32-128+ cores
  - 80-350W TDP

**Networking and Edge Infrastructure**
- 5G
- Mid core count, mid power switch and SmartNIC CPUs
  - 12-36 cores
  - 30-80W TDP

**5G Infrastructure**
- 5G
- Low core count, low power gateway and router CPUs
  - 4-16 cores
  - 20-35W TDP

**Arm Neoverse Cloud-to-Edge Workload Positioning**
- Neoverse V1
- Neoverse N2
- Neoverse E1
Arm Neoverse Scalable Compute Platforms

Arm CPU
- Neoverse N1, N2, V1

Arm SoC
- Coherent Mesh Network (CMN)
- GIC, MMU Virtualization
- Power Control Kit
- CryptosIsland Secure Enclave

Backplane
- GIC, MMU Virtualization
- CryptosIsland Secure Enclave
- Power Control Kit
- DDR
- PCIe/CXL
- Custom Accelerators

Memory
- DDR4
- DDR5
- HBM

IO
- PCIe
- CCIX
- CXL
- GbE

CMN

Common Software Platform, SBSA, SBBR, Arm SystemReady SR
Arm Architecture v8.x-A, AMBA

Everything in green and blue boxes provided by Arm
Marvell OCTEON 10 DPU family

- Up to 400 GE
- Network ports Ethernet
- Packet parser
- Up to 400 GE

Arm Neoverse N2 compute

- Host CPU (x86 or Arm) Application
- Hardware packet accelerators

OCTEON 10 performance specifications

- Compute: Up to 36 N2 cores, 1000+ SPECint
- TSMC 5nm
- Datapath: 400G+
- Ethernet ports: Up to 400GE
- AI/ML: 100’s TOPS
- Security: 400G+ of IPSEC and SSL

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*Spec CPU ® 2006 estimated
Arm Neoverse N2... Coming Soon in Silicon

**Marvell OCTEON 10 Family**

**Compute**
- Up to 36 Neoverse N2 cores
- SPECint > 1000

**Accelerators**
- Inline ML engine
- Inline IPSec
- SSL/TLS
- Vector packet processing (VPP)

**SW**
- DPDK networking suite for Control, Management and Fast path stacks
- SDK with Linux kernel and user plane extensions

**Memory**
- DDR5-5200 + ECC on-board memory

**I/O**
- Up to 400GE
- Integrated 1Terabit switch
- PCIe 5.0

Available in Q4
Arm Neoverse N2: Arm’s First v9 Implementation

**Datapath**
- Large system extensions (Atomics)
- Int8 dot product instructions
  - RCpc memory ordering
- Scalable vector extension (SVE, SVE2)
- FP round to constrained int.
- Javascript FP conversion
- Enh. cond. flag manipulation
- Complex number support
  - Bfloat16
- Int8 matmul

**Security and Crypto**
- Privileged and Stage2 Access-Never
- Unprivileged access override
- Side-channel protection
- SHA512, SHA3, SM3, SM4
  - Data independent instructions timing mode
- Branch target identification
- Speculation control
- RAS extensions
- Pointer authentication
- Secure EL2

**Telemetry and system management**
- Support for persistent memory
- HW update of access/dirty bits
- Enhanced PMU
  - MPAM
- Deep persistence support
  - Self-hosted trace
- Embedded trace extension

**Virtualization**
- 16-bits VMID
- Virtual host extension (type2 hyp)
  - Nested virtualization
- TLB maintenance ops
  - Small page tables
- Enhanced virtualization traps

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Arm Neoverse N2: Core Implementation
Major push in efficient performance over Neoverse N1

+40% IPC performance uplift

- Micro-architectural improvements across the board
- Improves benchmarks and server workloads
- Maintains similar power- and area-efficiency as N1, maximizes perf/Watt
Arm Neoverse N2: Core Implementation

Neoverse N2 maintains the same perf efficiency trajectory as Neoverse N1

**Neoverse N1**

On 7nm node:
- 1.0-1.8W / core+L2
- 1.15-1.4 mm² core + L2 (512K/1M L2)

**Neoverse N2**

On 5nm node:
- 1.0-2.0W / core+L2
- 1.1-1.3 mm² core + L2 (512K/1M L2)
- Max core freq 3.6GHz

*Pictures not to scale*
## Neoverse N2 Core Pipeline Upgrades: Front-End

<table>
<thead>
<tr>
<th>Branch Prediction</th>
<th>Neoverse N1</th>
<th>Neoverse N2</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Branch Prediction Width</td>
<td>8 instrs</td>
<td>2 x 8 instrs (up to 2 taken per cycle)</td>
<td>2x</td>
</tr>
<tr>
<td>Nano BTB (0 cyc taken-branch bubble)</td>
<td>16 entry</td>
<td>64 entry</td>
<td>4x</td>
</tr>
<tr>
<td>Conditional branch direction state</td>
<td>1x</td>
<td>1.5x</td>
<td>1.5x</td>
</tr>
<tr>
<td>Main BTB</td>
<td>6K entry</td>
<td>8K entry</td>
<td>1.33x</td>
</tr>
<tr>
<td>Alt-Path Branch Prediction</td>
<td>No</td>
<td>Yes</td>
<td>New</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fetch</th>
<th>Neoverse N1</th>
<th>Neoverse N2</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 Instruction cache</td>
<td>64KB</td>
<td>64KB</td>
<td>-</td>
</tr>
<tr>
<td>Mop Cache</td>
<td>N/A</td>
<td>1.5K entry</td>
<td>New</td>
</tr>
<tr>
<td>Fetch Queue</td>
<td>12-entry</td>
<td>16-entry</td>
<td>1.33x</td>
</tr>
<tr>
<td>Fetch Width</td>
<td>4 instr</td>
<td>4 instr from I$, 5 instr from MOP$</td>
<td>Up to 1.5x</td>
</tr>
<tr>
<td>Early branch redirect</td>
<td>Yes (unconditional)</td>
<td>Yes (uncond + cond)</td>
<td>Improved feature</td>
</tr>
<tr>
<td>Decode width</td>
<td>4 (I-cache)</td>
<td>4 (I-cache) or 5 (Mop cache)</td>
<td>Up to 1.25x</td>
</tr>
</tbody>
</table>
Arm Neoverse N2: Front-End
Re-design front-end microarchitecture to achieve higher performance and security

- Higher fetch bandwidth and lower latency
  - Branch predict up to 16-inst/cycle, 2-taken/cycle
  - New Macro-op (MOP) cache with 1.5k entries
- More accurate branch predictor:
  - 50% larger branch direction predictor

- More efficient instruction handling:
  - More instruction fusion via MOP cache
  - Special effort to accelerate application with large code footprints
    - Improved Branch Predictor Directed Prefetch by larger fetch queue for more outstanding requests
    - 33% larger BTB with shorter average latency
    - Early re-steering for conditional branches that miss the BTB
- Enhanced security:
  - Branch target is tagged by software context number (SCXTNUM, Arm v8.5)

Lower branch misprediction and lower I-cache miss penalty for server workloads
## Neoverse N2 Core Pipeline Upgrades: Mid-Core & Back-End

<table>
<thead>
<tr>
<th></th>
<th>Neoverse N1</th>
<th>Neoverse N2</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mid-Core</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rename width</td>
<td>4 instrs</td>
<td>5 instrs</td>
<td>1.2x</td>
</tr>
<tr>
<td>Rename Checkpointing</td>
<td>N</td>
<td>Y</td>
<td><strong>New</strong></td>
</tr>
<tr>
<td>ROB size</td>
<td>128</td>
<td>160+</td>
<td>1.25x</td>
</tr>
<tr>
<td>ALUs</td>
<td>3</td>
<td>4</td>
<td>1.33x</td>
</tr>
<tr>
<td>Branch resolution</td>
<td>1 per cycle</td>
<td>2 per cycle</td>
<td>2x</td>
</tr>
<tr>
<td>Overall Pipeline Depth</td>
<td>11 cycles</td>
<td>10 cycles</td>
<td>1.1x</td>
</tr>
<tr>
<td><strong>Back-End</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L1 Data cache</td>
<td>64KB</td>
<td>64KB</td>
<td>-</td>
</tr>
<tr>
<td>L2 Cache</td>
<td>Private 512KB / 1MB</td>
<td>Private 512KB / 1MB</td>
<td>-</td>
</tr>
<tr>
<td>AGUs</td>
<td>2-LD/ST</td>
<td>2-LD/ST + 1 LD</td>
<td>1.5x</td>
</tr>
<tr>
<td>L1 LD Hit bandwidth</td>
<td>2x 16B/cycle</td>
<td>3x 16B/cycle</td>
<td>1.5x</td>
</tr>
<tr>
<td>Store data B/W</td>
<td>16B / cycle</td>
<td>32B / cycle</td>
<td>2x</td>
</tr>
<tr>
<td>L2 bandwidth</td>
<td>32B read + 32B write</td>
<td>64B read + 64B write</td>
<td>2x</td>
</tr>
<tr>
<td>L2 Transactions</td>
<td>48</td>
<td>64</td>
<td>1.3x</td>
</tr>
<tr>
<td>Data Prefetch Engines</td>
<td>Stride, spatial/region and stream</td>
<td>N1 + temporal, stride, and tablewalk improvements</td>
<td><strong>New and improved</strong></td>
</tr>
</tbody>
</table>
Arm Neoverse N2: Prefetchers and Caches

Correlated Miss Caching (CMC) prefetching

- Temporal prefetcher can prefetch arbitrary, repeating access patterns to accelerate workloads with temporal streams, such as pointer chasing.

- Records hard to predict memory patterns that the prefetcher can leverage when needed.

- This technology can significantly reduce load-to-use latency and increase the leverage on the L2 cache.
Arm Neoverse N2 IPC Performance Uplift vs. Neoverse N1
ISO-frequency, unconstrained memory subsystem, single core

Mix of SPEC CPU® components, industry benchmarks and server/networking workloads

- SPEC CPU 2006 (est.)
- SPEC CPU 2017 (est.)

32% IPC improvement vs Neoverse N1

Nginx Reverse Proxy

Performance is estimated for SPEC CPU®2006 and SPEC CPU®2017
Multichip and CXL Leadership for the Intelligent Era

CMN-700 enables next-gen use cases for multi-chip, memory expansion and accelerators

Tightly Coupled Heterogeneous Compute

Coherent In-package Chiplets

Coherent Multi-Socket

Memory Expansion & Pooling

Coherent Accelerator

Coherent Multichip Link (CML)

Coherent Express Link (CXL)

GPU

NPU
Arm Neoverse CMN-700

- **Step Function in Performance on Every Vector**
  - Larger mesh, double wide channels
  - 3x increased cross-sectional BW
  - Hot spot reroute capability
  - CHI enhancements for optimized data movement
  - Upgraded IO bandwidth (PCIe Gen 5)

- **Composability for a Customized Datacenter**
  - CXL host, device and memory expansion support
  - Enables homogeneous and heterogeneous topologies
  - Optimized multi-protocol gateway (CXL and CML)

<table>
<thead>
<tr>
<th>Platform Capabilities</th>
<th>CMN-600</th>
<th>CMN-700</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td># cores supported per die / system</td>
<td>64¹ / 128</td>
<td>256 / 512</td>
<td>4x</td>
</tr>
<tr>
<td>System Level Cache (SLC) size per die</td>
<td>128MB</td>
<td>512MB</td>
<td>4x</td>
</tr>
<tr>
<td>Nodes (cross points) per die</td>
<td>64 (8x8)</td>
<td>144 (12x12)</td>
<td>2.25x</td>
</tr>
<tr>
<td># memory device ports (ex, DRAM, HBM) per die</td>
<td>16</td>
<td>40</td>
<td>2.5x</td>
</tr>
<tr>
<td>Multichip ports per die</td>
<td>4</td>
<td>32</td>
<td>8x</td>
</tr>
</tbody>
</table>

1. Indicates number of cores directly connected per die; higher core counts can be achieved using a core aggregation layer (CAL)
Composable Datacenter SoCs

Example multi-die SoC with Super Home Node

Super Home Node Functions and Composability

- Home node for local memory
  - System level cache (SLC)
- Cluster cache for remote homed memory
  - Local coherency node and cache (LCC)
- Can be configured as Unified (SLC+LCC) or Decoupled (LCC and SLC)

Composability (Multichip and CXL attached)

- Unified SLC+LCC for **Homogeneous compute**
- Decoupled LCC for compute chiplets and HNF/SLC in **Heterogeneous Hub & Spoke**
- Home Node for CXL Host attached memory and LCC for Host managed Device memory (HDM)
- CXL Device Coherency Node (DCOH) for CXL Device

Homogeneous Compute

- Performance optimized

Heterogeneous Hub & Spoke

- Flexible and re-use optimized
MPAM: Memory Partitioning and Monitoring

MPAM bounds and monitors process interaction/interference in shared resources

- All memory requests issued by Processing Elements in the system are decorated with MPAM information:
  - Neoverse Cores
  - IO Devices can use the SMMU v3.2 or default MPAM values
- SW can measure resource usage matching two fields:
  - PARTID & PMG – Partition IDs and Perf Monitor Group
    - PMG can be used to probe whether a certain application within a PARTID should have its own PARTID
  - For Memory BW, read and write bandwidth are assessed independently
  - Can independently monitor memory requests for code and data – can have separate PARTIDs and PMGs
- Memory System Components provide controls for capacity or bandwidth
CBusy: Scalable and Sustainable Performance

Memory bandwidth management is paramount to extract optimal and predictable performance on high core count, high performance systems.

Completer Busy (CBusy)
- Automatic regulation of CPU prefetch requests based on system congestion
- CPU aggregates and filters feedback from system
- Feedback affects hardware prefetcher aggressiveness
- CPU can also throttle its maximum outstanding transactions
- MPAM aware CBusy for VM based bandwidth control
CBusy: Dynamic Prefetcher Throttling

Neoverse N2 cores support four levels of prefetcher aggressiveness:

- The most aggressive mode can generate prefetches with as low as 20% accuracy
- The most conservative mode will target 100% accuracy

When surplus bandwidth is available, more conservative prefetching results in significant performance loss (shown in orange in the graph)

When memory BW is highly contended, higher performance can be achieved by avoiding more aggressive, less accurate prefetches

CBusy dynamically tunes prefetcher aggressiveness based on BW available, often resulting in best performance (shown in blue in the graph)
Arm Neoverse N2: Performance Without Compromise

Hyper-threading won the datacenter, per-thread performance will win the cloud

- Arm Neoverse N2 Edge 32c, 32t
- Arm Neoverse N1 64c, 64t
- Traditional 2020 24c, 48t
- Traditional 2021 40c, 80t
- Traditional 2020 64c, 128t
- Traditional 2021 64c, 128t
- Arm Neoverse N2 Cloud 128c, 128t

Neoverse N2 Cloud: 128 cores, 3.0GHz, 8xDDR5-4800
Neoverse N2 Edge: 32 cores, 2.7GHz, 4xDDR4-3200

Traditional 2020 is measured by Arm
Traditional 2021 data is projected by Arm
Arm Neoverse performance data is estimated by Arm
Arm Neoverse N2: Relentless Improvements on Real Workloads

ISO process/frequency/core count (8 cores), Neoverse N2 significantly outperforms N1

MemcacheD: 133%
MySQL: 129%
NGINX: 148%

Approximate projections on reduced workload configurations on pre-silicon models. Server configuration under test limited to 8 cores for both configurations. Performance on silicon systems is subjected to change due to different SW configurations and partners’ choices on HW implementations.
Arm Neoverse N2: Cloud-to-Edge Perf-per-Watt Leadership

- Comprehensively upgraded microarchitecture delivers +40% IPC uplift over Neoverse N1 at ISO process & frequency
- First Armv9 core supporting SVE2, Arm’s state-of-the-art vector ISA
- Continues Arm industry leadership in performance / watt
- Up to 256-cores and 512MB of system-level cache per die
- Coming soon from Arm’s partners who have the design freedom to add custom acceleration and tune system configurations for market leadership
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End Notes

Slide Title: Arm Neoverse N2: Performance Without Compromise

- Traditional 24c/48t CPU is Intel Xeon 8268
- Traditional 64c/128t CPU is AMD EPYC 7742
- Traditional next 40c/80t CPU is projected on a 40 core Intel Ice Lake system
- Traditional next 64c/128t CPU is projected on AMD EPYC 7763
- SMT and Turbo are enabled for measurements on both x86 SKUs
- GCC-snapshot-10. 2.1- fsf-10.100, 2MB Page size, unless noted otherwise
- Compiler Flags for Neoverse N1: -march=armv8.2-a+crypto -O3 -ftree-vectorize -ffast-math
- Compiler Flags for Neoverse N2: -march=armv8.6-a+crypto+fp16+dotprod+sve -O3 -ftree-vectorize -ffast-math
- Compiler Flags for Traditional systems: -mcpu=native -O3 -ftree-vectorize -ffast-math
Thank You!